

# DS26528DK Octal T1/E1/J1 Transceiver Design Kit Daughter Card

[www.maxim-ic.com](http://www.maxim-ic.com)

## GENERAL DESCRIPTION

The DS26528DK is an easy-to-use evaluation board for the DS26528 octal T1/E1/J1 single-chip transceiver (SCT). The DS26528DK is intended to be used as a daughter card with either the DK2000 or the DK101 (included) motherboards. The board comes complete with a DS26528 SCT, transformers, termination resistors, configuration switches, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

Each DS26528DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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## DESIGN KIT CONTENTS

DS26528DK Daughter Card  
 DK101 Low-Cost Motherboard  
 CD\_ROM Including:  
   ChipView Software  
   DS26528DK Data Sheet  
   DK101 Data Sheet  
   DS26528 Data Sheet  
   DS26528 Errata Sheet (if applicable)

## FEATURES

- Demonstrates Key Functions of DS26528 T1/E1/J1 SCT
- Includes DS26528 SCT, Transformers, BNC and RJ48 Network Connectors, and Termination Passives
- BNC Connections for 75Ω E1
- RJ48 Connectors for 120Ω E1 and 100Ω T1
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21354 Register Set
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-Of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

## ORDERING INFORMATION

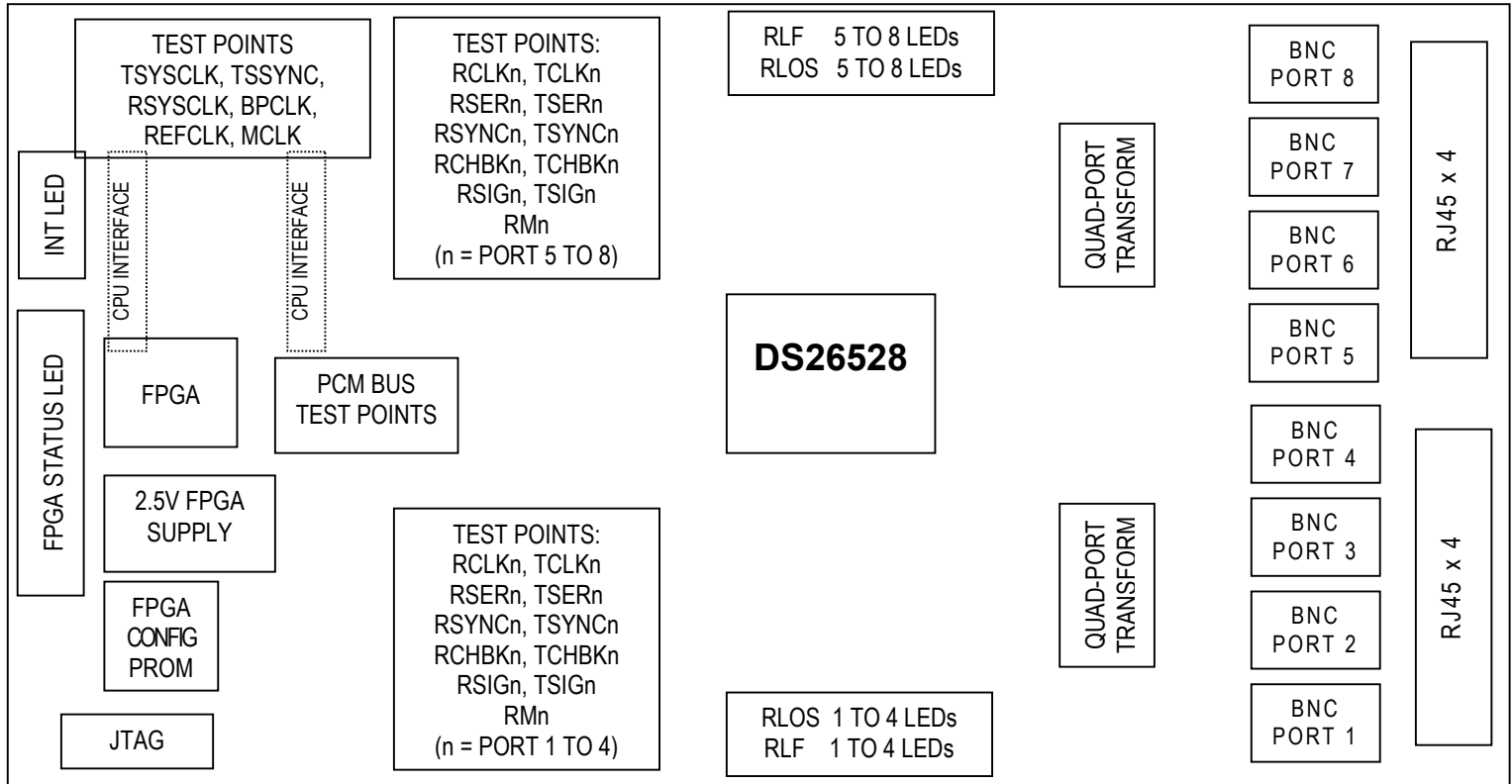
| PART      | DESCRIPTION  |
|-----------|--|
| DS26528DK | DS26528 Demo Kit Daughter Card (with included DK101 Motherboard) |



## COMPONENT LIST

| DESIGNATION  | QTY | DESCRIPTION   | SUPPLIER              | PART               |
|--|-----|---|-----------------------|--------------------|
| C1–C5, C7, C8, C9, C20, C21, C29–C32, C35, C40, C41, C43, C49, C50, C59, C60 | 22  | 1 $\mu$ F 10%, 16V ceramic capacitors (1206)                                | Panasonic             | ECJ-3YB1C105K      |
| C6, C10–C18, C24, C33, C36–C39, C42, C44–C48                                 | 22  | 0.1 $\mu$ F 20%, 16V X7R ceramic capacitors (0603)                          | Arrow                 | 0603YC104MAT2      |
| C19, C22, C23, C25–C28, C34, C61, C62  | 10  | 10 $\mu$ F 20%, 10V ceramic capacitors (1206)                               | Panasonic             | ECJ-3YB1A106M      |
| C51–C58  | 8   | 0.1 $\mu$ F 10%, 25V ceramic capacitors (1206)                              | Panasonic             | ECJ-3VB1E104K      |
| C63–C70  | 8   | 560pF 5%, 50V ceramic capacitors (1206)                                     | Digi-Key              | 478-1489-2-ND      |
| D1   | 1   | L_DIODE 1A, 50V general-purpose silicon                                     | General Semiconductor | 1N4001             |
| DS1  | 1   | L_LED, GREEN, SMD   | Panasonic             | LN1351C            |
| DS2–DS18   | 17  | LED, RED, SMD   | Panasonic             | LN1251C            |
| J1   | 1   | L_TERMINAL strip, 10-pin, dual-row, vertical                                | Samtec                | TSW-105-07-T-D     |
| J2–J9  | 8   | 22-pin headers, dual row, vertical  | Samtec                | HDR-TSW-111-14-T-D |
| J10–J25  | 16  | L_5-pin, 75 $\Omega$ vertical BNC connectors                                | Cambridge             | CP-BNCP-004        |
| J26, J27   | 2   | Right-angle RJ45 8-pin, 4-port jack   | Molex                 | 43223-8140         |
| J28, J29   | 2   | 50-pin, dual-row, vertical SMD sockets                                      | Samtec                | TFM-125-02-S-D-LC  |
| JP1  | 1   | 12-pin, dual-row, vertical connector  | Digi-Key              | S2012-06-ND        |
| JP2, JP3, JP5–JP8  | 6   | 100-mil, 2 pos jumper<br>Not populated                                      | Labstock              | Not populated      |
| JP4  | 1   | 12-pin, dual row, vertical connector<br>Not populated                       | Digi-Key              | S2012-06-ND        |
| R1–R32   | 32  | 0 $\Omega$ 5%, 1/8W resistors (1206)  | Panasonic             | ERJ-8GEYJ0R00V     |
| R33  | 1   | L_RES 330 $\Omega$ 5%, 1/16W resistors (0603)                               | Panasonic             | ERJ-3GEYJ331V      |
| R34, R35, R39–R54  | 18  | 330 $\Omega$ 5%, 1/10W resistors (0805)                                     | Panasonic             | ERJ-6GEYJ331V      |
| R36, R38, R55  | 3   | 10k $\Omega$ 5%, 1/16W resistors (0603)                                     | Panasonic             | ERJ-3GEYJ103V      |
| R37  | 1   | 30 $\Omega$ 5%, 1/10W resistor (0805)                                       | Panasonic             | ERJ-6GEYJ300V      |
| R56–R71  | 16  | 61.9 $\Omega$ 1%, 1/8W resistors (1206)                                     | Panasonic             | ERJ-8ENF61R9V      |
| R72–R79  | 8   | L_RES 51.1 $\Omega$ 1%, 1/10W resistors (0805)<br>(ok to substitute for 5%) | Panasonic             | ERJ-6ENF51R1V      |
| SW1–SW8  | 8   | 6-pin, DPDT, through-hole slide switches                                    | Tyco                  | SSA22              |
| T1, T2   | 2   | XFMR, XMIT/RCV, 1 to 2 and 1 to 1, SMT 32-pin                               | Pulse Engineering     | TX1475             |
| U1   | 1   | 8-Pin $\mu$ MAX/SO<br>2.5V or Adj   | Maxim                 | MAX1792EUA25       |
| U2   | 1   | 1Mb flash-based config mem  | Xilinx                | XCF01SV020C        |
| U3   | 1   | Xilinx Spartan 2.5V FPGA, 256-pin BGA                                       | Xilinx                | XC2S50-5FG256C     |
| U4   | 1   | 256-pin BGA octal transceiver<br>(0 $^{\circ}$ C to +70 $^{\circ}$ C)       | Dallas Semiconductor  | DS26528            |

## BOARD FLOORPLAN



## PC BOARD ERRATA

- The mode pins of the FPGA were incorrectly connected, which affects FPGA configuration. The hardware modifications to correct this are not ideal, as the FPGA is in a race condition during power-up. The FPGA requires a fast slew rate on  $V_{CC}$  during power-up. After power-up the LED DS1 will light green if FPGA configuration is successful. If the DS1 LED does not light green, cycle power by removing and reattaching the  $V_{CC}$  banana plug. The removal/reattach of the  $V_{CC}$  banana plug results in a faster slew rate on  $V_{CC}$  than simply cycling the power supply.

## BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at [www.maxim-ic.com/DS26528DK](http://www.maxim-ic.com/DS26528DK) QuickView data sheet for these files.

## HARDWARE CONFIGURATION

### Using the DK101 Processor Board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V. (The external 5V connector is unused. Additionally, the “TIM 5V supply” headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the Flash programming switch, which should be OFF.
- From the Programs menu launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

### Using the DK2000 Processor Board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply may be connected to connector J2.
- From the Programs menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

### General:

- Upon power-up the RLOS LEDs (red) will be lit, the INT LED (red) will not be lit, and the FPGA Status LED (DS1 green) will be lit. (See the *PC Board Errata* section note regarding FPGA power-up configuration on page 3).
- When using BNC network connections, slide SW1–SW8 such that the BNC shell is grounded (indicated by the PC board silkscreen). When using RJ45 network connections, slide SW1–SW8 such that the BNC shell is not grounded (indicated by the PC board silkscreen).

## QUICK SETUP (REGISTER VIEW)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
- The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the *\_DS26528DK01A0\_FPGA.def*. Note: Through the “links” section this will also load the DS26528 global def file along with eight LIU def files and eight framer def files.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS26528.
- Predefined register settings for several functions are available as initialization files.
  - .ini files are loaded by selecting the menu **F**ile→**R**eg Ini File→**L**oad Ini File.
  - Load the .ini file *E1\_75ohmLiu\_impMatchOn.ini*.
  - After loading the .ini file, the following may be observed:
    - The RLOS LEDs extinguishes upon external loopback.
    - The DS26528 is in E1 mode with impedance match on and begins transmitting AIS.

### Miscellaneous:

- Clock frequencies, port-to-port connection, and certain pin bias levels are provided by a register-mapped FPGA that is on the DS26528 daughter card.
- The definition file for this FPGA is named *DS26528DC\_FPGA.def*. The FPGA register map definitions are located on page 6. A drop-down menu on the right of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked “BASIC OPERATION.”

## ADDRESS MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given in the following table(s) are relative to the beginning of the daughter card address space (shown above).

**Table 1. Daughter Card Address Map**

| OFFSET           | DEVICE  | DESCRIPTION                                   |
|------------------|---------|---|
| 0X0000 to 0X0087 | FPGA    | Board identification and clock/signal routing |
| 0X1000 to 0X10EF | DS26528 | DS26528 Framer 1 Rx registers                 |
| 0X10F0 to 0X10FF | DS26528 | DS26528 Global registers                      |
| 0X1100 to 0X11EF | DS26528 | DS26528 Framer 1 Tx registers                 |
| 0X11F0 to 0X11FF | DS26528 | DS26528 reserved registers                    |
| 0X1200 to 0X1FFF | DS26528 | DS26528 Framer 2 to 8 registers               |
| 0X2000 to 0X20FF | DS26528 | DS26528 LIU 1 to 8 registers                  |
| 0X2100 to 0X217F | DS26528 | DS26528 BERT 1 to 8 registers                 |
| 0X2180 to 0X2FFF | DS26528 | DS26528 reserved registers                    |

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named "DS26528DC\_FPGA.def."

## FPGA Register Map

**Table 2. FPGA Register Map**

| OFFSET | REGISTER NAME            | TYPE      | DESCRIPTION                            |
|--------|--------------------------|-----------|--|
| 0X0000 | BID                      | Read only | Board ID                               |
| 0X0002 | XBIDH                    | Read only | High Nibble Extended Board ID          |
| 0X0003 | XBIDM                    | Read only | Middle Nibble Extended Board ID        |
| 0X0004 | XBIDL                    | Read only | Low Nibble Extended Board ID           |
| 0X0005 | BREV                     | Read only | Board FAB Revision                     |
| 0X0006 | AREV                     | Read only | Board Assembly Revision                |
| 0X0007 | PREV                     | Read only | PLD Revision                           |
| 0X0010 | PINSET                   | Control   | DS26528 Configuration Pin Settings     |
| 0X0011 | CSR                      | Control   | DS26528 MCLK and REFCLKIO Source       |
| 0X0012 | SYSCLK_TR                | Control   | DS26528 Tx and Rx SYSCLK Source        |
| 0X0013 | SYNCTSS                  | Control   | DS26528 TSSYNC Source                  |
| 0X0014 | TCSRn<br>(n = 8 to 1)    | Control   | DS26528 TCLK Source, Ports 8–1         |
| 0X0024 |                          |           |  |
| 0X0034 |                          |           |  |
| 0X0044 |                          |           |  |
| 0X0054 |                          |           |  |
| 0X0064 |                          |           |  |
| 0X0074 |                          |           |  |
| 0X0084 |                          |           |  |
| 0X0015 | TSYNCSn<br>(n = 8 to 1)  | Control   | DS26528 TSYNC Source, Ports 8–1        |
| 0X0025 |                          |           |  |
| 0X0035 |                          |           |  |
| 0X0045 |                          |           |  |
| 0X0055 |                          |           |  |
| 0X0065 |                          |           |  |
| 0X0075 |                          |           |  |
| 0X0085 |                          |           |  |
| 0X0016 | RSYNCSRn<br>(n = 8 to 1) | Control   | DS26528 RSYNC Source Select, Ports 8–1 |
| 0X0026 |                          |           |  |
| 0X0036 |                          |           |  |
| 0X0046 |                          |           |  |
| 0X0056 |                          |           |  |
| 0X0066 |                          |           |  |
| 0X0076 |                          |           |  |
| 0X0086 |                          |           |  |
| 0X0017 | TSERSRn<br>(n = 8 to 1)  | Control   | DS26528 TSER Source, Ports 8–1         |
| 0X0027 |                          |           |  |
| 0X0037 |                          |           |  |
| 0X0047 |                          |           |  |
| 0X0057 |                          |           |  |
| 0X0067 |                          |           |  |
| 0X0077 |                          |           |  |
| 0X0087 |                          |           |  |
| 0X0018 | PRSER                    | Control   | PCM RSER Source                        |
| 0X0019 | PSYNC                    | Control   | PCM RSYNC/TSYNC Source                 |
| 0X001A | PCLK                     | Control   | PCM RCLK/TCLK Source                   |

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## ID REGISTERS

**BID: BOARD ID (Offset=0X0000)**

BID is read only with a value of 0xD.

**XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset=0X0002)**

XBIDH is read only with a value of 0x0.

**XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset=0X0003)**

XBIDM is read only with a value of 0x1.

**XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset=0X0004)**

XBIDL is read only with a value of 0x6.

**BREV: BOARD FAB REVISION (Offset=0X0005)**

BREV is read only and displays the current fab revision.

**AREV: BOARD ASSEMBLY REVISION (Offset=0X0006)**

AREV is read only and displays the current assembly revision.

**PREV: PLD REVISION (Offset=0X0007)**

PREV is read only and displays the current PLD firmware revision.

## CONTROL REGISTERS

Register Name: **PINSET**

Register Description: **DS26528 Configuration Pin Settings**

Register Offset: **0x0010**

| Bit #   | 7 | 6 | 5 | 4 | 3    | 2      | 1      | 0       |
|---------|---|---|---|---|------|--------|--------|---------|
| Name    | — | — | — | — | TXEN | SCANMO | SCANEN | DIGIOEN |
| Default | — | — | — | — | 1    | 0      | 0      | 1       |

### Bit 3: DS26528 TXEN PIN

0 = Drive DS26528 TX ENABLE pin Low (Tri-state TTIP and TRING)

1 = Drive DS26528 TX ENABLE pin High (Normal operation, drive TTIP and TRING with data)

### Bit 2: DS26528 SCANMO PIN

0 = Drive DS26528 SCAN MODE pin Low (Normal operation)

1 = Drive DS26528 SCAN MODE pin High

### Bit 1: DS26528 SCANEN PIN

0 = Drive DS26528 SCAN ENABLE pin Low (Normal operation)

1 = Drive DS26528 SCAN ENABLE pin High

### Bit 0: DS26528 DIGIOEN PIN

0 = Drive DS26528 DIGIO ENABLE pin Low (Tri-state all DS26528 pins, if JTRST is low)

1 = Drive DS26528 DIGIO ENABLE pin High (Normal operation)

Register Name: **CSR**

Register Description: **DS26528 MCLK and REFCLKIO Source**

Register Offset: **0x0011**

| Bit #   | 7      | 6      | 5 | 4 | 3 | 2 | 1     | 0     |
|---------|--------|--------|---|---|---|---|-------|-------|
| Name    | RCSRC1 | RCSRC0 | — | — | — | — | MSRC1 | MSRC0 |
| Default | 1      | 1      | — | — | — | — | 0     | 1     |

### Bits 7 and 6: DS26528 REFCLKIO Source (RCSRC[1:0])

REFCLKIO Connection is defined in Table 3.

**Table 3. REFCLKIO Source Definition**

| RCSRC1, RCSRC0 | REFCLKIO CONNECTION                    |
|----------------|--|
| 00             | Drive REFCLKIO with the 1.544MHz clock |
| 01             | Drive REFCLKIO with the 2.048MHz clock |
| 1x             | Tri-state REFCLKIO                     |

### Bits 1 and 0: DS26528 MCLK Source (MSRC[1:0])

MCLK Connection is defined in Table 4.

**Table 4. MCLK Source Definition**

| MSRC1, MSRC0 | MCLK CONNECTION                    |
|--------------|------------------------------------|
| 00           | Drive MCLK with the 1.544MHz clock |
| 01           | Drive MCLK with the 2.048MHz clock |
| 1x           | Tri-state MCLK                     |



Register Name: **SYCLK\_TR**

Register Description: **DS26528 TSYCLK and RSYCLK Source**

Register Offset: **0x0012**

| Bit #   | 7   | 6   | 5 | 4 | 3 | 2 | 1   | 0   |
|---------|-----|-----|---|---|---|---|-----|-----|
| Name    | RS1 | RS0 | — | — | — | — | TS1 | TS0 |
| Default | 0   | 1   | — | — | — | — | 0   | 1   |

**Bits 7 and 6: DS26528 Port 4 RSYCLK Source (RS1, RS0)**

The source for RSYCLK 4 is defined as shown in Table 5.

**Table 5. RSYCLK Source Definition**

| RS1, RS0 | RSYCLK CONNECTION                    |
|----------|--------------------------------------|
| 00       | Drive RSYCLK with the 1.544MHz clock |
| 01       | Drive RSYCLK with the 2.048MHz clock |
| 10       | Drive RSYCLK with 8.192MHz clock     |
| 11       | Drive RSYCLK with DS26528 port BPCLK |

**Bits 1 and 0: DS26528 Port 1 TSYCLK Source (TS1, TS0)**

The source for TSYCLK is defined as shown in Table 6.

**Table 6. TSYCLK Source Definition**

| TS1, TS0 | TSYCLK CONNECTION                    |
|----------|--------------------------------------|
| 00       | Drive TSYCLK with the 1.544MHz clock |
| 01       | Drive TSYCLK with the 2.048MHz clock |
| 10       | Drive TSYCLK with 8.192MHz clock     |
| 11       | Drive TSYCLK with DS26528 port BPCLK |

Register Name: **SYNCTSS**

Register Description: **DS26528 TSSYNC Source**

Register Offset: **0x0013**

| Bit #   | 7 | 6 | 5 | 4 | 3     | 2     | 1     | 0     |
|---------|---|---|---|---|-------|-------|-------|-------|
| Name    | — | — | — | — | TSRC3 | TSRC2 | TSRC1 | TSRC0 |
| Default | — | — | — | — | 0     | 0     | 0     | 0     |

**Bit 3 to 0: DS26528 TSSYNC Source Select (TSRC[3:0])**

The source for TSSYNC is defined below.

| TSRC3–TSRC0 | TSSYNC SOURCE DEFINITION  |
|-------------|---|
| 0000        | Not using transmit-side elastic store, tri-state FPGA pin connected to TSSYNC (weak pulldown) |
| 0001        | Drive TSSYNC with RSYNC 1   |
| 0010        | Drive TSSYNC with RSYNC 2   |
| 0011        | Drive TSSYNC with RSYNC 3   |
| 0100        | Drive TSSYNC with RSYNC 4   |
| 0101        | Drive TSSYNC with RSYNC 5   |
| 0110        | Drive TSSYNC with RSYNC 6   |
| 0111        | Drive TSSYNC with RSYNC 7   |
| 1000        | Drive TSSYNC with RSYNC 8   |

**Note:** When driving TSSYNC with RSYNCx, the corresponding DS26528 port should be configured such that RSYNCx is an output (RIOCR.2 = 0).

Register Name: **TCSRn (n = 8 to 1)**

Register Description: **DS26528 TCLK Source Ports 8–1**

Register Offset: **0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084,**

| Bit #   | 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
|---------|---|---|---|---|----------|----------|----------|----------|
| Name    | — | — | — | — | TDS3     | TDS2     | TDS1     | TDS0     |
| Default | — | — | — | — | See note | See note | See note | See note |

#### Bits 3 to 0: DS26528 Port 1 TCLK Source (TDS[3:0])

| TDS3–TDS0 | TCLKx SOURCE DEFINITION             |
|-----------|-------------------------------------|
| 0000      | Tri-state TCLKx                     |
| 0001      | Drive TCLKx with RCLK1              |
| 0010      | Drive TCLKx with RCLK2              |
| 0011      | Drive TCLKx with RCLK3              |
| 0100      | Drive TCLKx with RCLK4              |
| 0101      | Drive TCLKx with RCLK5              |
| 0110      | Drive TCLKx with RCLK6              |
| 0111      | Drive TCLKx with RCLK7              |
| 1000      | Drive TCLKx with RCLK8              |
| 1001      | Drive TCLKx with the 1.544MHz clock |
| 1010      | Drive TCLKx with the 2.048MHz clock |

**Note:** Initial values are such that  $TCLK1 \leftarrow RCLK1$ ,  $TCLK2 \leftarrow RCLK2$ ,  $TCLK3 \leftarrow RCLK3$ ,  $TCLK4 \leftarrow RCLK4$ ,  $TCLK5 \leftarrow RCLK5$ ,  $TCLK6 \leftarrow RCLK6$ ,  $TCLK7 \leftarrow RCLK7$ ,  $TCLK8 \leftarrow RCLK8$ , which corresponds to address 0x14 = 0b0001, address 0x24 = 0b0010, address 0x34 = 0b0011, address 0x44 = 0b0100, address 0x54 = 0b0101, address 0x64 = 0b0110, address 0x74 = 0b0111 and address 0x84 = 0b1000.

Register Name: **TSYNCSn (n = 8 to 1)**

Register Description: **DS26528 TSYNC Source Ports 8–1**

Register Offset: **0x0015, 0x0025, 0x0035, 0x0045, 0x0055, 0x0065, 0x0075, 0x0085**

| Bit #   | 7 | 6 | 5 | 4 | 3     | 2     | 1     | 0     |
|---------|---|---|---|---|-------|-------|-------|-------|
| Name    | — | — | — | — | TSRC3 | TSRC2 | TSRC1 | TSRC0 |
| Default | — | — | — | — | 0     | 0     | 0     | 0     |

#### Bits 3 to 0: DS26528 Port 1 TSYNC Source (TSRC[3:0])

| TSRC3–TSRC | TSYNCx SOURCE DEFINITION |
|------------|--------------------------|
| 0000       | Tri-state TSYNCx         |
| 0001       | Drive TSYNCx with RSYNC1 |
| 0010       | Drive TSYNCx with RSYNC2 |
| 0011       | Drive TSYNCx with RSYNC3 |
| 0100       | Drive TSYNCx with RSYNC4 |
| 0101       | Drive TSYNCx with RSYNC5 |
| 0110       | Drive TSYNCx with RSYNC6 |
| 0111       | Drive TSYNCx with RSYNC7 |
| 1000       | Drive TSYNCx with RSYNC8 |

**Note:** When driving TSYNCx with RSYNCx, the corresponding DS26528 port should be configured such that TSYNCx is an input (TIOCR.2 = 0) and RSYNCx is an output (RIOCR.2 = 0).

Register Name: **RSYNCSRn (n = 8 to 1)**

Register Description: **DS26528 RSYNC Source Select, Ports 8–1**

Register Offset: **0x0016, 0x0026, 0x0036, 0x0046, 0x0056, 0x0066, 0x0076, 0x0086**

| Bit #   | 7 | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
|---------|---|---|---|---|------|------|------|------|
| Name    | — | — | — | — | RIO3 | RIO2 | RIO1 | RIO0 |
| Default | — | — | — | — | 0    | 0    | 0    | 0    |

#### Bits 3 to 0: DS26528 Port 1 RSYNC Source (RIO[3:0])

| RIO3–RIO0 | RSYNCx SOURCE DEFINITION |
|-----------|--------------------------|
| 0000      | Tri-state RSYNCx         |
| 0001      | Drive RSYNCx with RSYNC1 |
| 0010      | Drive RSYNCx with RSYNC2 |
| 0011      | Drive RSYNCx with RSYNC3 |
| 0100      | Drive RSYNCx with RSYNC4 |
| 0101      | Drive RSYNCx with RSYNC5 |
| 0110      | Drive RSYNCx with RSYNC6 |
| 0111      | Drive RSYNCx with RSYNC7 |
| 1000      | Drive RSYNCx with RSYNC8 |

**Note:** When driving RSYNCy with RSYNCx, the corresponding DS26528 port should be configured such that RSYNCx is an output (RIOCR.2 = 0) and RSYNCy is an input (RIOCR.2 = 1).

Register Name: **TSERSRn (n = 8 to 1)**

Register Description: **DS26528 TSER Source, Ports 8–1**

Register Offset: **0x0017, 0x0027, 0x0037, 0x0047, 0x0057, 0x0067, 0x0077, 0x0087**

|         |   |   |   |   |          |          |          |          |
|---------|---|---|---|---|----------|----------|----------|----------|
| Bit #   | 7 | 6 | 5 | 4 | 3        | 2        | 1        | 0        |
| Name    | — | — | — | — | TS3      | TS2      | TS1      | TS0      |
| Default | — | — | — | — | See note | See note | See note | See note |

**Bits 3 to 0: DS26528 Port 1 TSER Source (TSRC[3:0])**

| TS3–TS0 | TSERx SOURCE DEFINITION            |
|---------|------------------------------------|
| 0000    | Tri-state TSERx                    |
| 0001    | Drive TSERx with RSER1             |
| 0010    | Drive TSERx with RSER2             |
| 0011    | Drive TSERx with RSER3             |
| 0100    | Drive TSERx with RSER4             |
| 0101    | Drive TSERx with RSER5             |
| 0110    | Drive TSERx with RSER6             |
| 0111    | Drive TSERx with RSER7             |
| 1000    | Drive TSERx with RSER8             |
| 1001    | Drive TSERx with data from PCM bus |

**Note:** Initial values are such that  $TSER1 \leftarrow RSER1$ ,  $TSER2 \leftarrow RSER2$ ,  $TSER3 \leftarrow RSER3$ ,  $TSER4 \leftarrow RSER4$ ,  $TSER5 \leftarrow RSER5$ ,  $TSER6 \leftarrow RSER6$ ,  $TSER7 \leftarrow RSER7$ ,  $TSER8 \leftarrow RSER8$ , which corresponds to address 0x17 = 0b0001, address 0x27 = 0b0010, address 0x37 = 0b0011, address 0x47 = 0b0100, address 0x57 = 0b0101, address 0x67 = 0b0110, address 0x77 = 0b0111 and address 0x87 = 0b1000.

Register Name: **PRSER**  
 Register Description: **PCM RSER Source**  
 Register Offset: **0x0018**

| Bit #   | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Name    | R8EN | R7EN | R6EN | R5EN | R4EN | R3EN | R2EN | R1EN |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Note:** The PRSER register is for use with the DK2000 only.

**Bit 7: PCM RSER Source (R8EN)**

0 = Do not drive DS26528 Port 8 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 8 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 6: PCM RSER Source (R7EN)**

0 = Do not drive DS26528 Port 7 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 7 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 5: PCM RSER Source (R6EN)**

0 = Do not drive DS26528 Port 6 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 6 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 4: PCM RSER Source (R5EN)**

0 = Do not drive DS26528 Port 5 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 5 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 3: DS26528 PCM RSER Source (R4EN)**

0 = Do not drive DS26528 Port 4 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 4 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 2: PCM RSER Source (R3EN)**

0 = Do not drive DS26528 Port 3 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 3 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 1: PCM RSER Source (R2EN)**

0 = Do not drive DS26528 Port 2 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 2 RSER with selected other RSER pins and drive onto PCM\_RSER

**Bit 0: PCM RSER Source (R1EN)**

0 = Do not drive DS26528 Port 1 RSER onto PCM\_RSER

1 = Logically OR DS26528 Port 1 RSER with selected other RSER pins and drive onto PCM\_RSER

Register Name: **PSYNC**  
 Register Description: **PCM RSYNC/TSYNC Source**  
 Register Offset: **0x0019**

| Bit #   | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Name    | TSR3 | TSR2 | TSR1 | TSR0 | RSR3 | RSR2 | RSR1 | RSR0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

*Note: PSYNC register is for use with the DK2000 only.*

#### Bits 7 to 4: PCM\_TSYNC Source (TSR[3:0])

| TSR3–TSR0 | PCM_TSYNC SOURCE                            |
|-----------|---|
| 0000      | Tri-state PCM_TSYNC                         |
| 0001      | PCM_TSYNC is driven by DS26528 port 1 TSYNC |
| 0010      | PCM_TSYNC is driven by DS26528 port 2 TSYNC |
| 0011      | PCM_TSYNC is driven by DS26528 port 3 TSYNC |
| 0100      | PCM_TSYNC is driven by DS26528 port 4 TSYNC |
| 0101      | PCM_TSYNC is driven by DS26528 port 5 TSYNC |
| 0110      | PCM_TSYNC is driven by DS26528 port 6 TSYNC |
| 0111      | PCM_TSYNC is driven by DS26528 port 7 TSYNC |
| 1000      | PCM_TSYNC is driven by DS26528 port 8 TSYNC |

#### Bits 3 to 0: PCM\_RSYNC Source (RSR[3:0])

| RSR3–RSR0 | PCM_RSYNC SOURCE                            |
|-----------|---|
| 0000      | Tri-state PCM_RSYNC                         |
| 0001      | PCM_RSYNC is driven by DS26528 port 1 RSYNC |
| 0010      | PCM_RSYNC is driven by DS26528 port 2 RSYNC |
| 0011      | PCM_RSYNC is driven by DS26528 port 3 RSYNC |
| 0100      | PCM_RSYNC is driven by DS26528 port 4 RSYNC |
| 0101      | PCM_RSYNC is driven by DS26528 port 5 RSYNC |
| 0110      | PCM_RSYNC is driven by DS26528 port 6 RSYNC |
| 0111      | PCM_RSYNC is driven by DS26528 port 7 RSYNC |
| 1000      | PCM_RSYNC is driven by DS26528 port 8 RSYNC |

Register Name: **PCLK**  
 Register Description: **PCM RCLK/TCLK Source**  
 Register Offset: **0x001A**

| Bit #   | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Name    | TSR3 | TSR2 | TSR1 | TSR0 | RSR3 | RSR2 | RSR1 | RSR0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

*Note: PCLK register is for use with the DK2000 only.*

#### Bits 7 to 4: PCM\_TCLK Source (TSR[3:0])

| TSR3—TSR0 | PCM_TCLK SOURCE   |
|-----------|---|
| 0000      | Tri-state PCM_TCLK pin at FPGA                            |
| 0001      | PCM_TCLK is driven by source used for DS26528 port 1 TCLK |
| 0010      | PCM_TCLK is driven by source used for DS26528 port 2 TCLK |
| 0011      | PCM_TCLK is driven by source used for DS26528 port 3 TCLK |
| 0100      | PCM_TCLK is driven by source used for DS26528 port 4 TCLK |
| 0101      | PCM_TCLK is driven by source used for DS26528 port 5 TCLK |
| 0110      | PCM_TCLK is driven by source used for DS26528 port 6 TCLK |
| 0111      | PCM_TCLK is driven by source used for DS26528 port 7 TCLK |
| 1000      | PCM_TCLK is driven by source used for DS26528 port 8 TCLK |
| 1001      | PCM_TCLK is driven by DS26528 BPCLK                       |

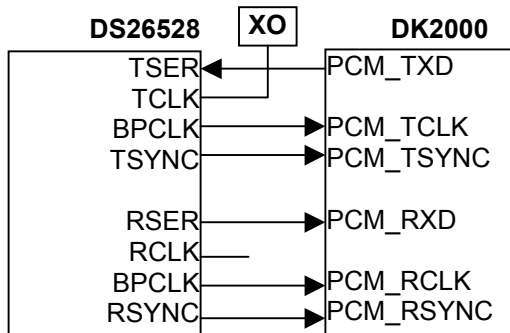
#### Bits 3 to 0: PCM\_RCLK Source (RSR[3:0])

| RSR3—RSR0 | PCM_RCLK SOURCE                           |
|-----------|---|
| 0000      | Tri-state PCM_RCLK pin at FPGA            |
| 0001      | PCM_RCLK is driven by DS26528 port 1 RCLK |
| 0010      | PCM_RCLK is driven by DS26528 port 2 RCLK |
| 0011      | PCM_RCLK is driven by DS26528 port 3 RCLK |
| 0100      | PCM_RCLK is driven by DS26528 port 4 RCLK |
| 0101      | PCM_RCLK is driven by DS26528 port 5 RCLK |
| 0110      | PCM_RCLK is driven by DS26528 port 6 RCLK |
| 0111      | PCM_RCLK is driven by DS26528 port 7 RCLK |
| 1000      | PCM_RCLK is driven by DS26528 port 8 RCLK |
| 1001      | PCM_RCLK is driven by DS26528 BPCLK       |



## FPGA CONTROL EXAMPLES

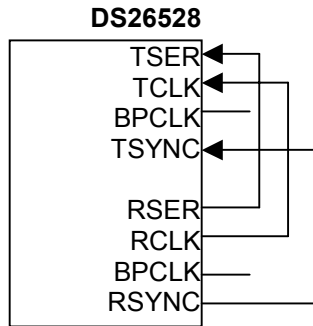
### Scenario #1: DS26528 to/from DK2000



**Table 7. FPGA Configuration for Scenario #1 (Port 1, T1 Mode)**

| REGISTER NAME | SETTING | COMMENT   |
|---------------|---------|---|
| CSR           | 0X01    | Drive DS26528 MCLK with 2.048MHz  |
| TCSR1         | 0X09    | Drive TCLK with 1.544MHz  |
| SYSCLK_TR     | 0X00    | Drive TSYSClk and RSYSClk with 1.544MHz   |
| TSYNCS1       | 0X00    | Tri-state FPGA driver pin for DS26528 TSYNC1  |
| SYNCTSS       | 0X01    | Drive TSSync with RSYNC1  |
| RSYNCSRn      | 0X00    | Tri-state FPGA driver pin for DS26528 RSYNC   |
| TSERSR1       | 0X09    | Drive DS26528 TSER1 with data from PCM bus  |
| PRSER         | 0X01    | Drive DS26528 RSER1 onto PCM bus  |
| PSYNC         | 0X11    | PCM RSYNC and PCM TSYNC are provided by DS26528 port 1 RSYNC and TSYNC (respectively) |
| PCLK          | 0X99    | PCM RCLK and TCLK are driven by port 1 BPCLK  |

**Scenario #2: External Remote Loopback  
(full bandwidth, not just payload)**



**Table 8. FPGA Configuration for Scenario #2 (Port 1, T1 Mode)**

| REGISTER NAME | SETTING | COMMENT                                     |
|---------------|---------|---|
| CSR           | 0X01    | Drive DS26528 MCLK with 2.048MHz            |
| TCSR1         | 0X01    | Drive TCLK1 with RCLK1                      |
| SYSCLK_TR     | 0X00    | Drive TSYCLK with 1.544MHz                  |
| TSYNCS1       | 0X01    | Drive TSYNC1 with RSYNC1                    |
| SYNCTSS       | 0X01    | Drive TSSYNC with RSYNC1                    |
| RSYNCSRN      | 0X00    | Tri-state FPGA driver pin for DS26528 RSYNC |
| TSERSR1       | 0X01    | Drive DS26528 TSER1 with data from RSER1    |
| PRSER         | NA      | Unused                                      |
| PSYNC         | NA      | Unused                                      |
| PCLK          | NA      | Unused                                      |

**Table 9. DS26528 Partial Configuration for Scenario #2 (Port 1, T1 Mode)**

| REGISTER NAME | SETTING   | COMMENT                         |
|---------------|-----------|---------------------------------|
| RIOCR         | RSIO = 0  | RSYNC is an output              |
| TIOCR         | TSIO = 0  | TSYNC is an input               |
| TESCR         | TESE = 0  | Bypass Rx and Tx elastic stores |
| RESCR         | RESE = 0  |                                 |
| TCR3          | TCSS1 = 0 | TCLK is driven by TCLK pin      |
|               | TCSS2 = 0 |                                 |

## DS26528 INFORMATION

For more information about the DS26528, consult the DS26528 data sheet available on our website at [www.maxim-ic.com/DS26528](http://www.maxim-ic.com/DS26528). Software downloads are also available for this design kit.

## DS26528DK INFORMATION

For more information about the DS26528DK, including software downloads, consult the DS26528DK data sheet available on our website at [www.maxim-ic.com/DS26528DK](http://www.maxim-ic.com/DS26528DK).

## TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

## SCHEMATICS

The DS26528DK schematics are featured in the following pages.

# DS26528

## OCTAL T1/E1/J1 TRANSCEIVER DESIGN KIT

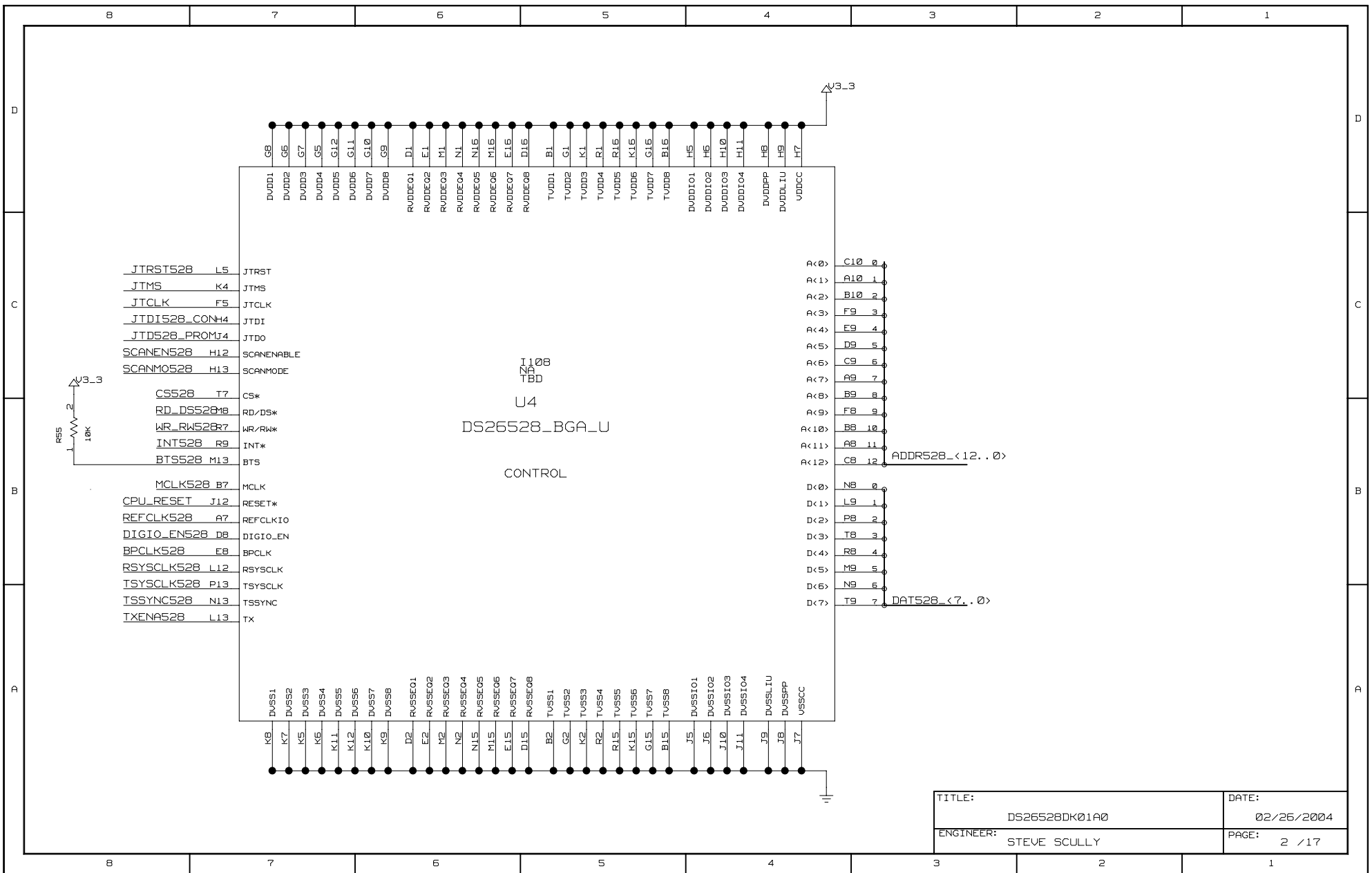
### CONTENTS

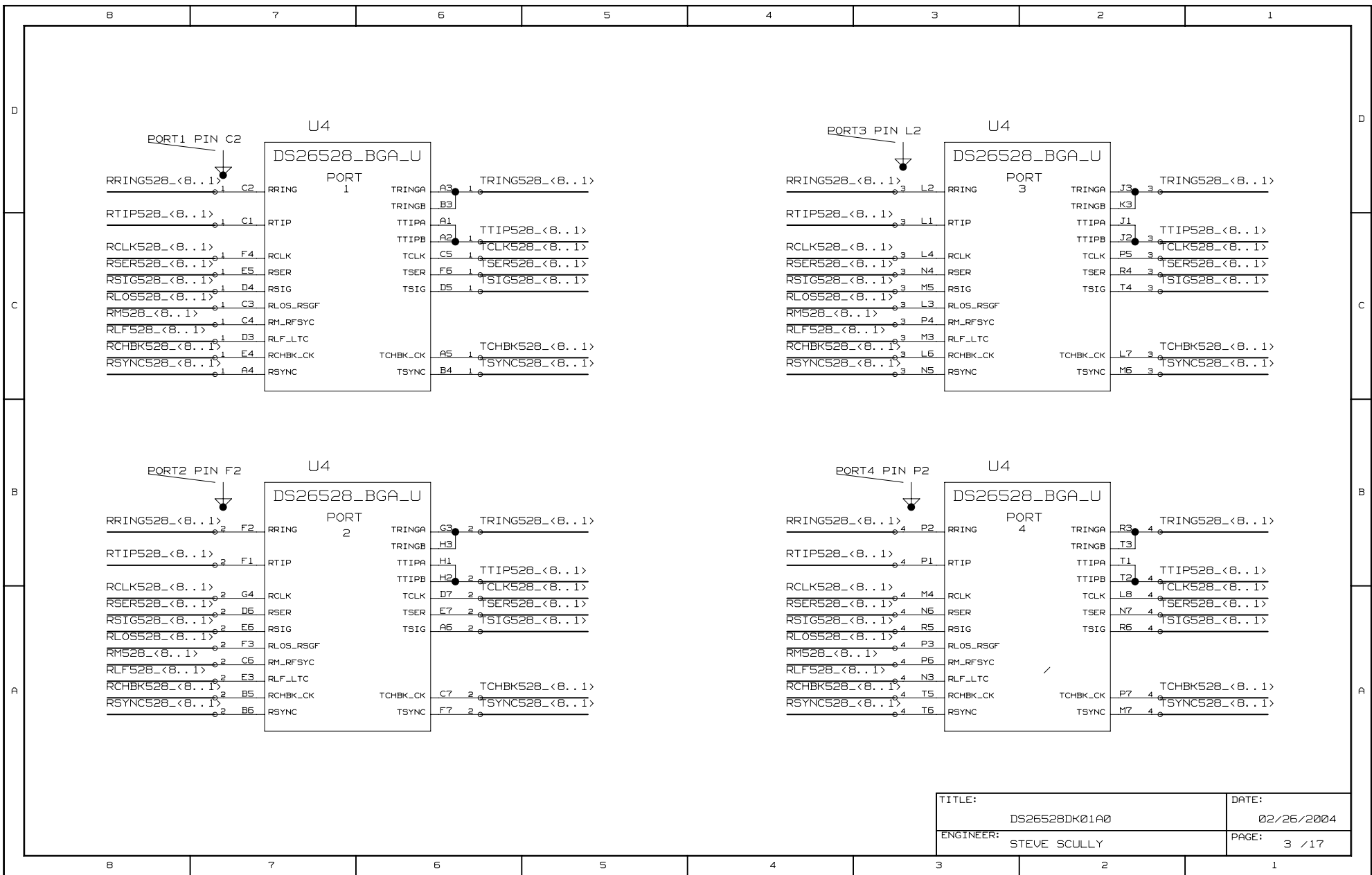
1. CONTENTS
2. DS26528 CONTROL
3. DS26528 PORTS 1-4
4. DS26528 PORTS 5-8
5. DS26528 BNC / XFRM 1-2
6. DS26528 BNC / XFRM 3-4
7. DS26528 BNC / XFRM 5-6
8. DS26528 BNC / XFRM 7-8
9. FPGA (SIGNAL MUX)
10. DS26528 TEST POINTS
11. PROCESSOR INTERFACE
12. FPGA ADDRESS DATA BUS
13. JTAG CHAIN - FPGA FLASH - VOLTAGE BOOST
14. FPGA CONTROL
15. DECOUPLING
16. CROSS REF NETLIST
17. CROSS REF PARTS

PCB ERRATA IS DOCUMENTED IN THE USER MANUAL

PRINTED: Mon Jun 28 19:06:49 2004

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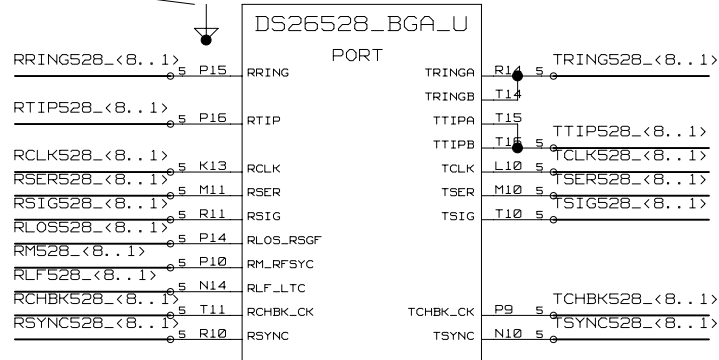
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8 7 6 5 4 3 2 1

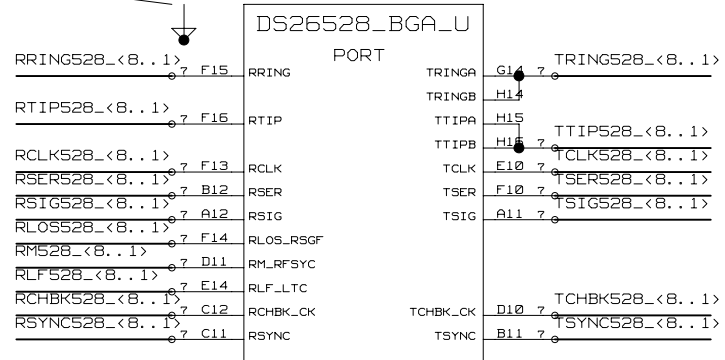
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D

PORT5 PIN P15 U4



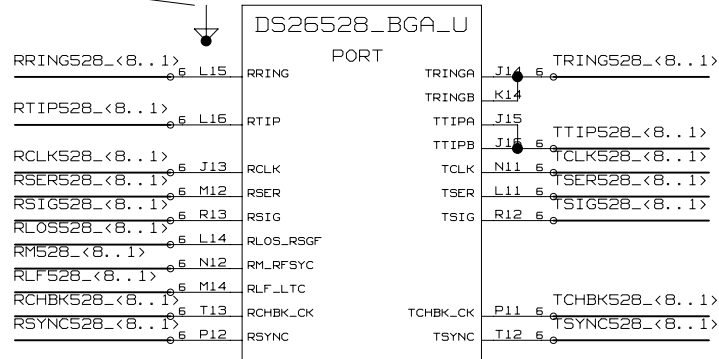
PORT7 PIN F15 U4



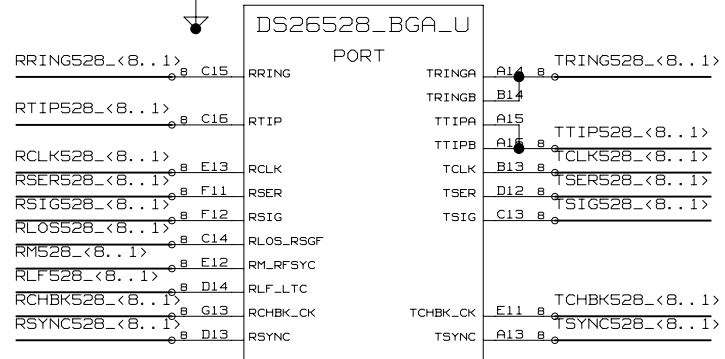
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C

PORT6 PIN L15 U4



PORT8 PIN C15 U4



B

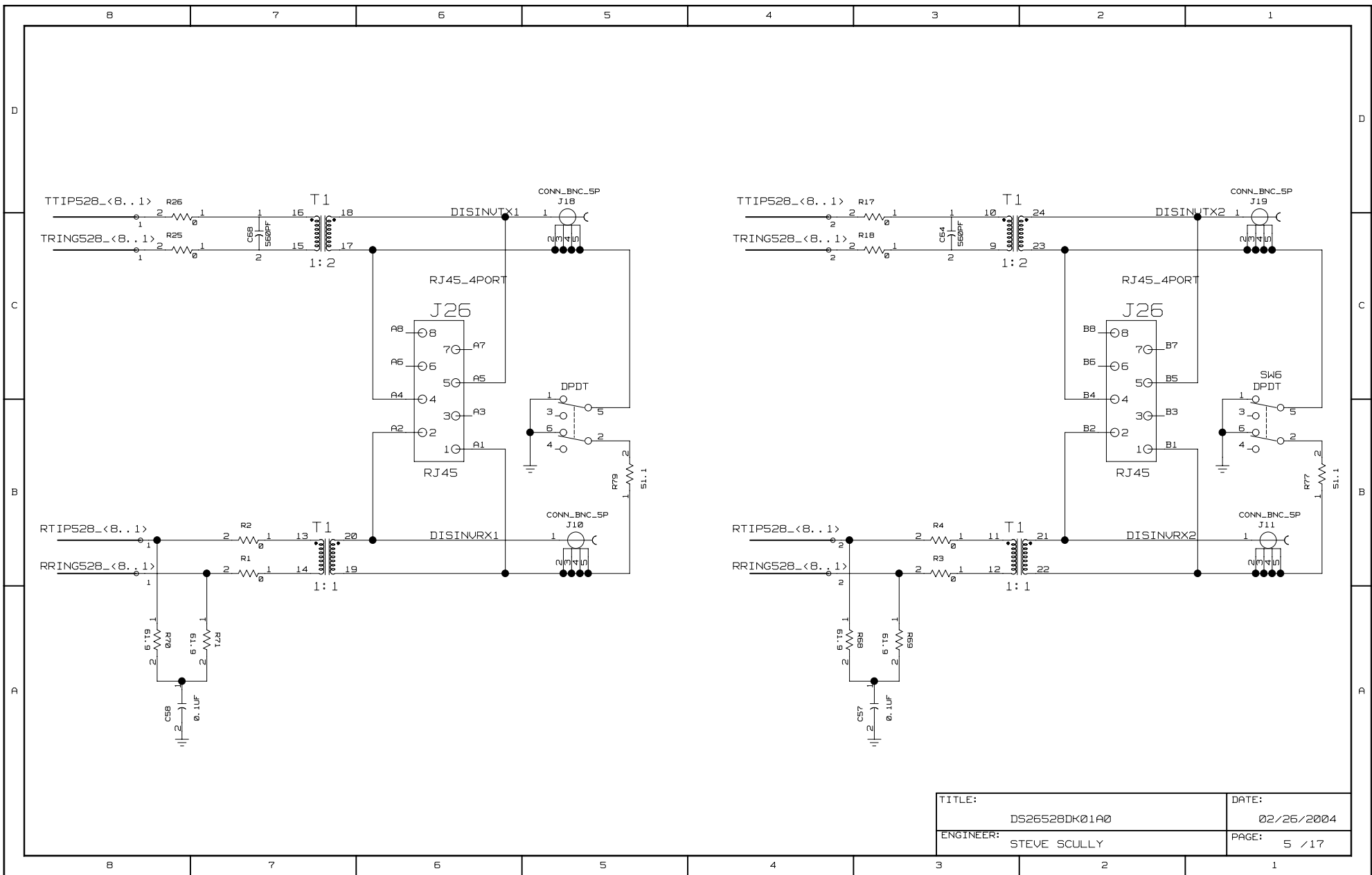
B

A

A

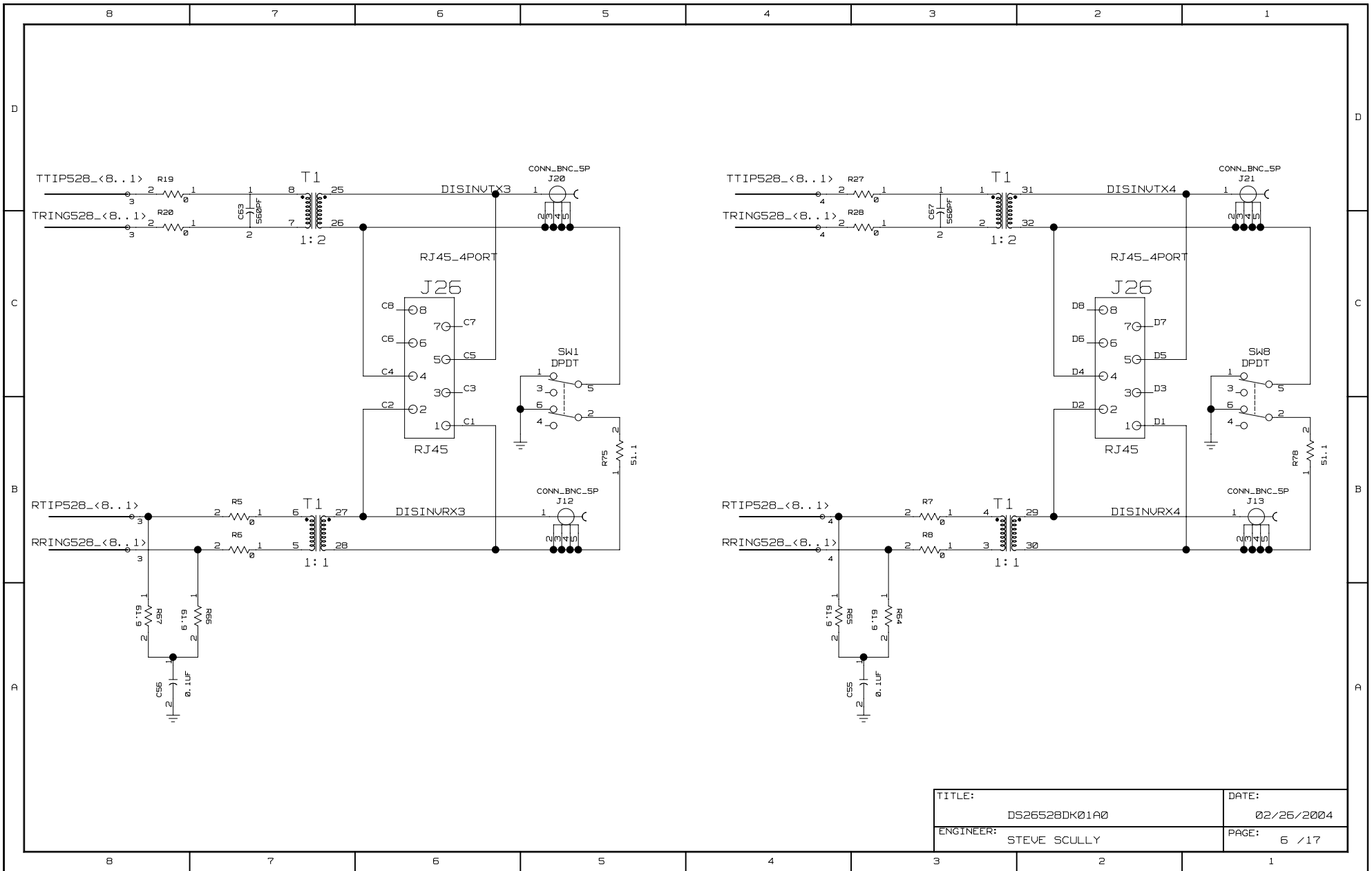
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8 7 6 5 4 3 2 1

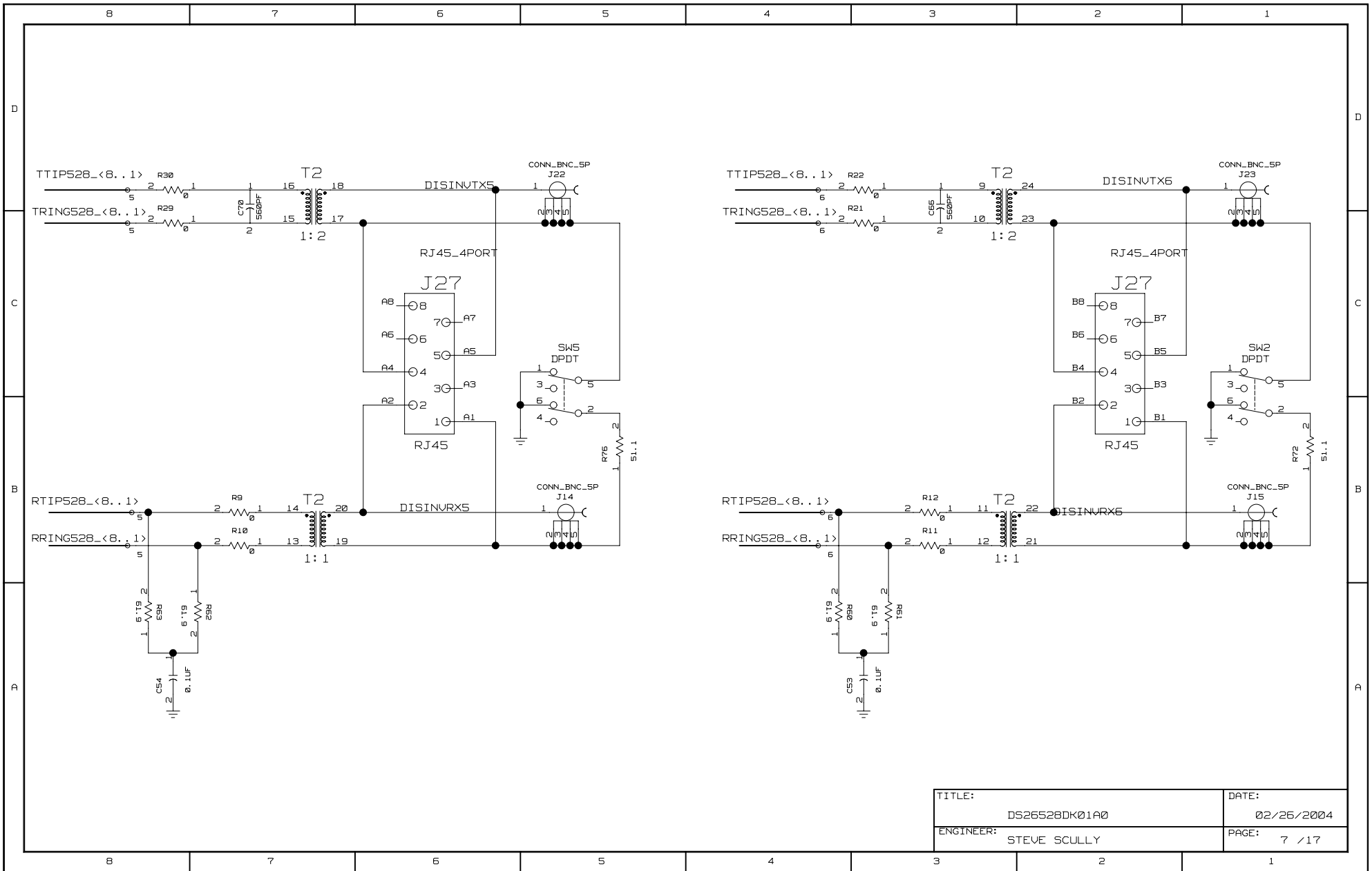


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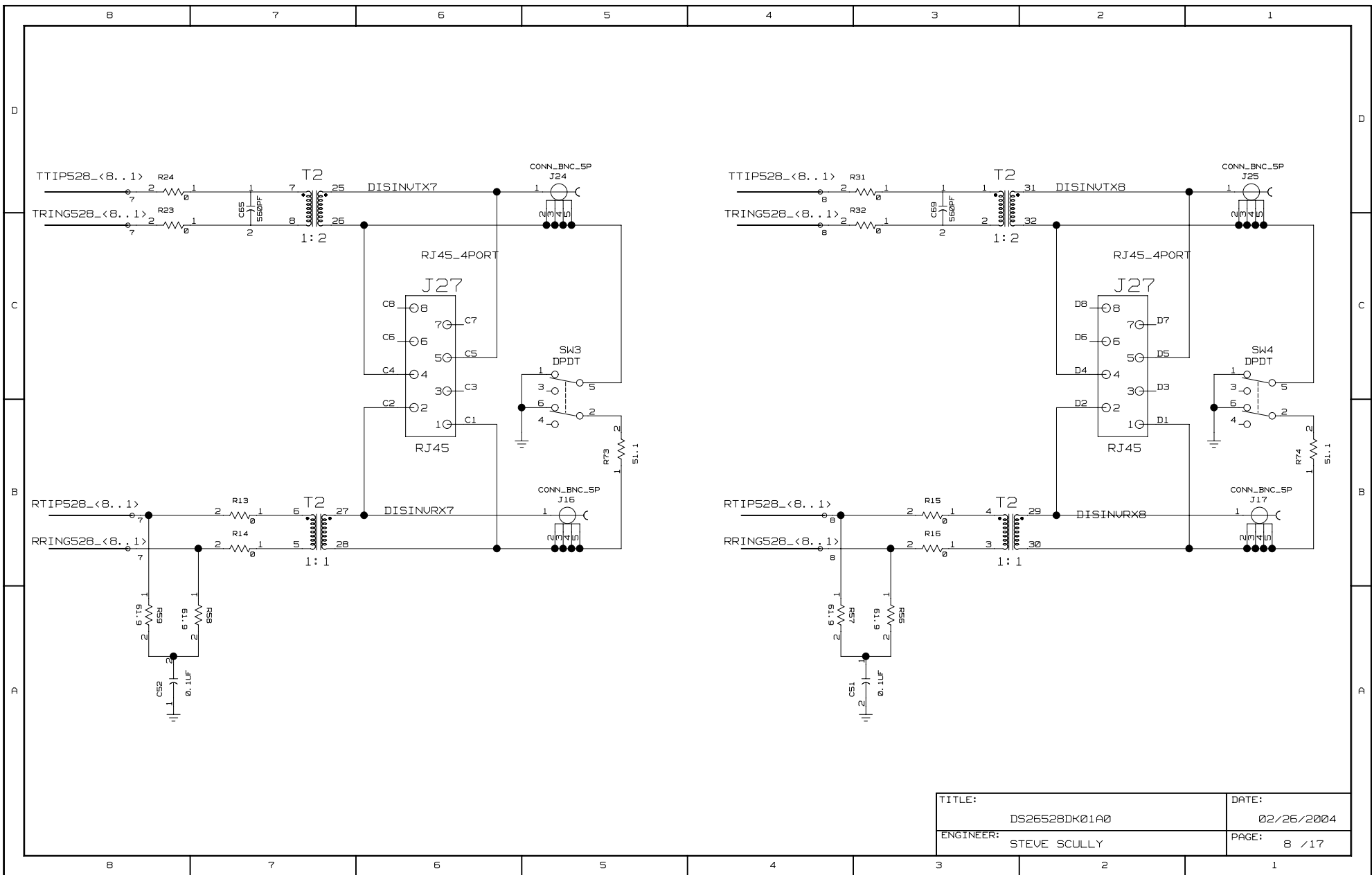




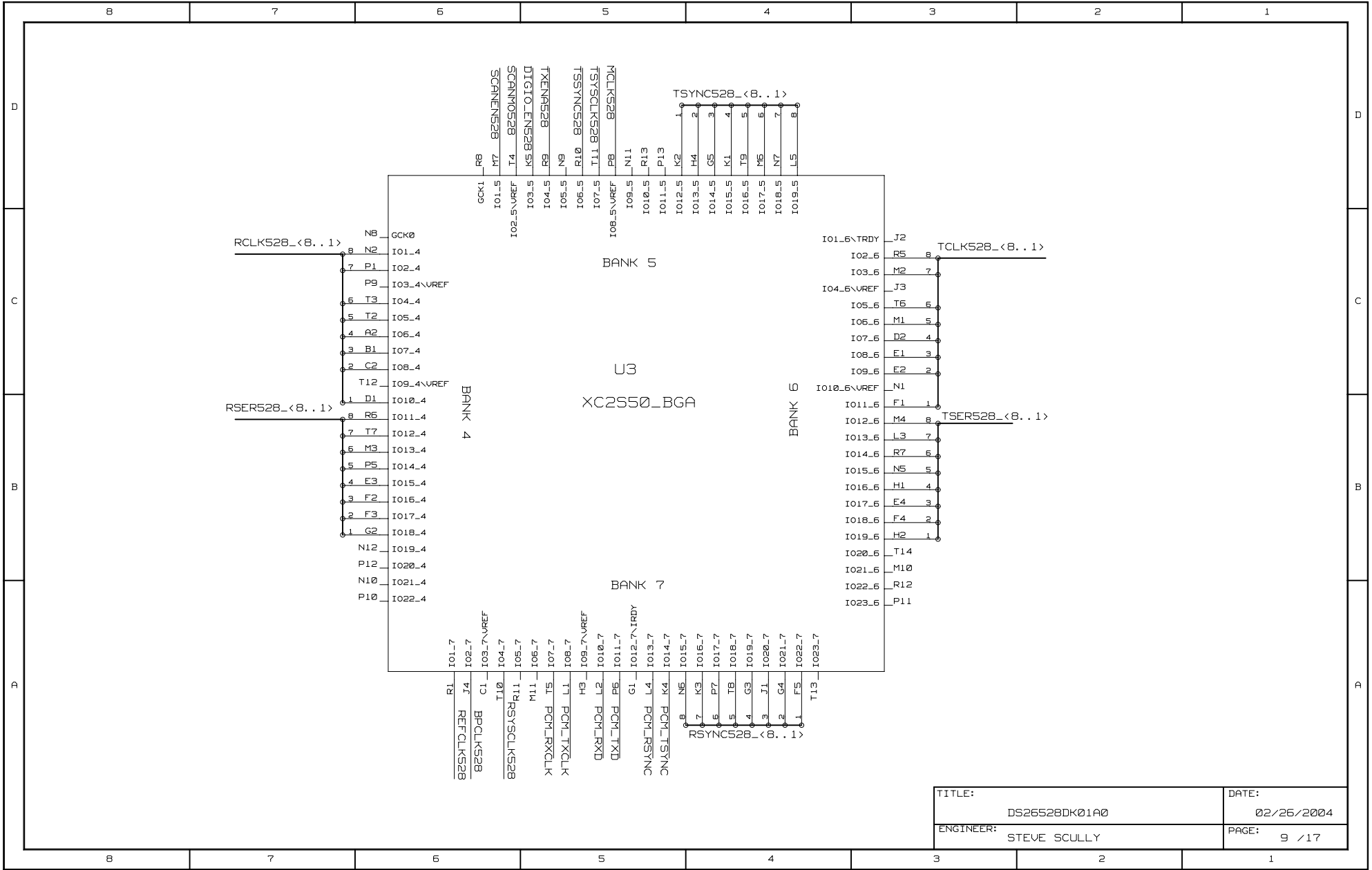
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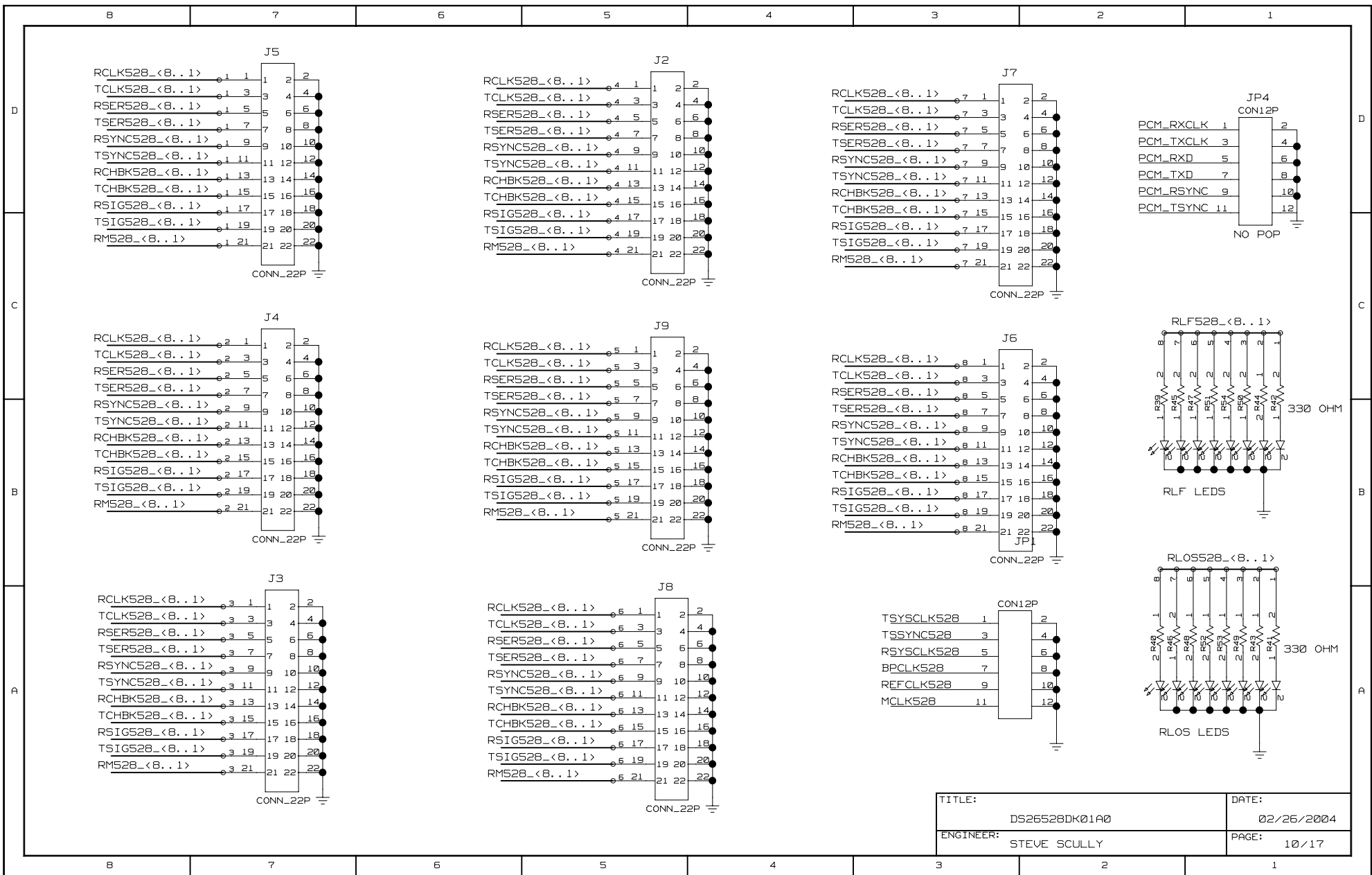
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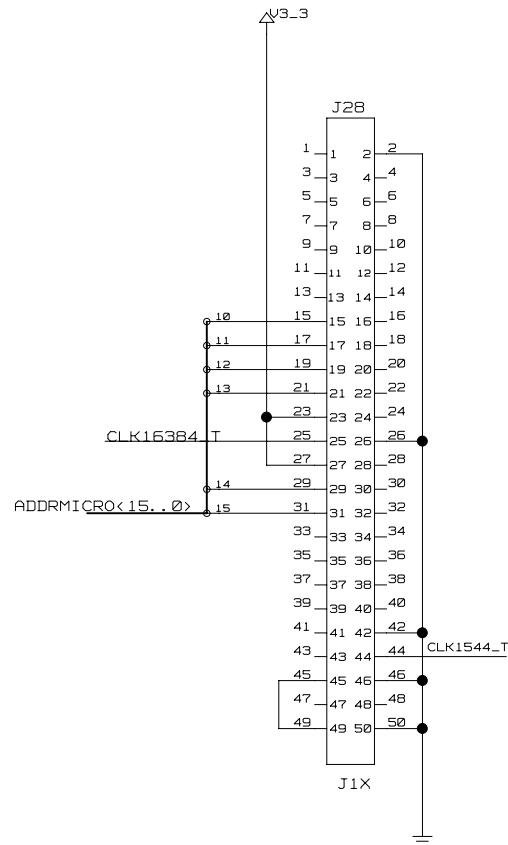
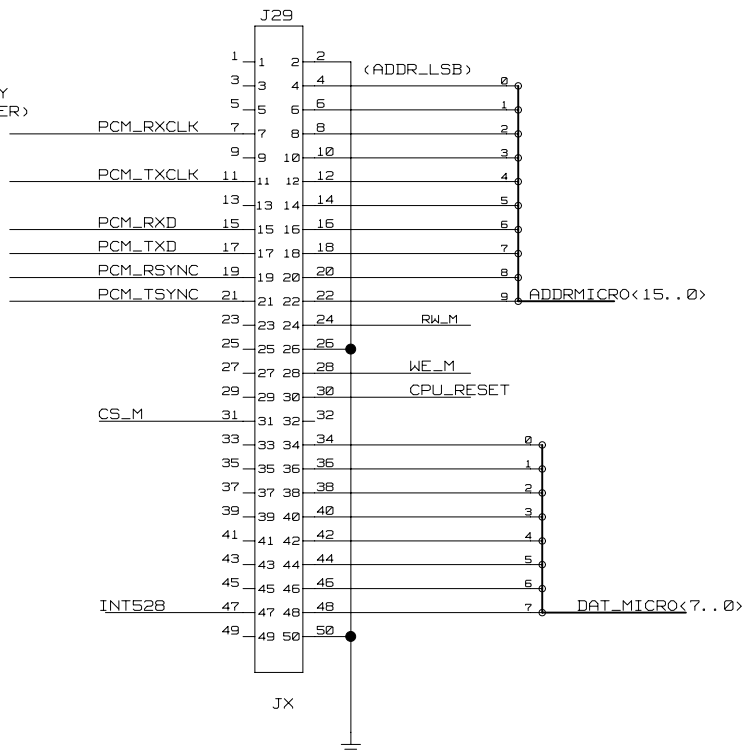
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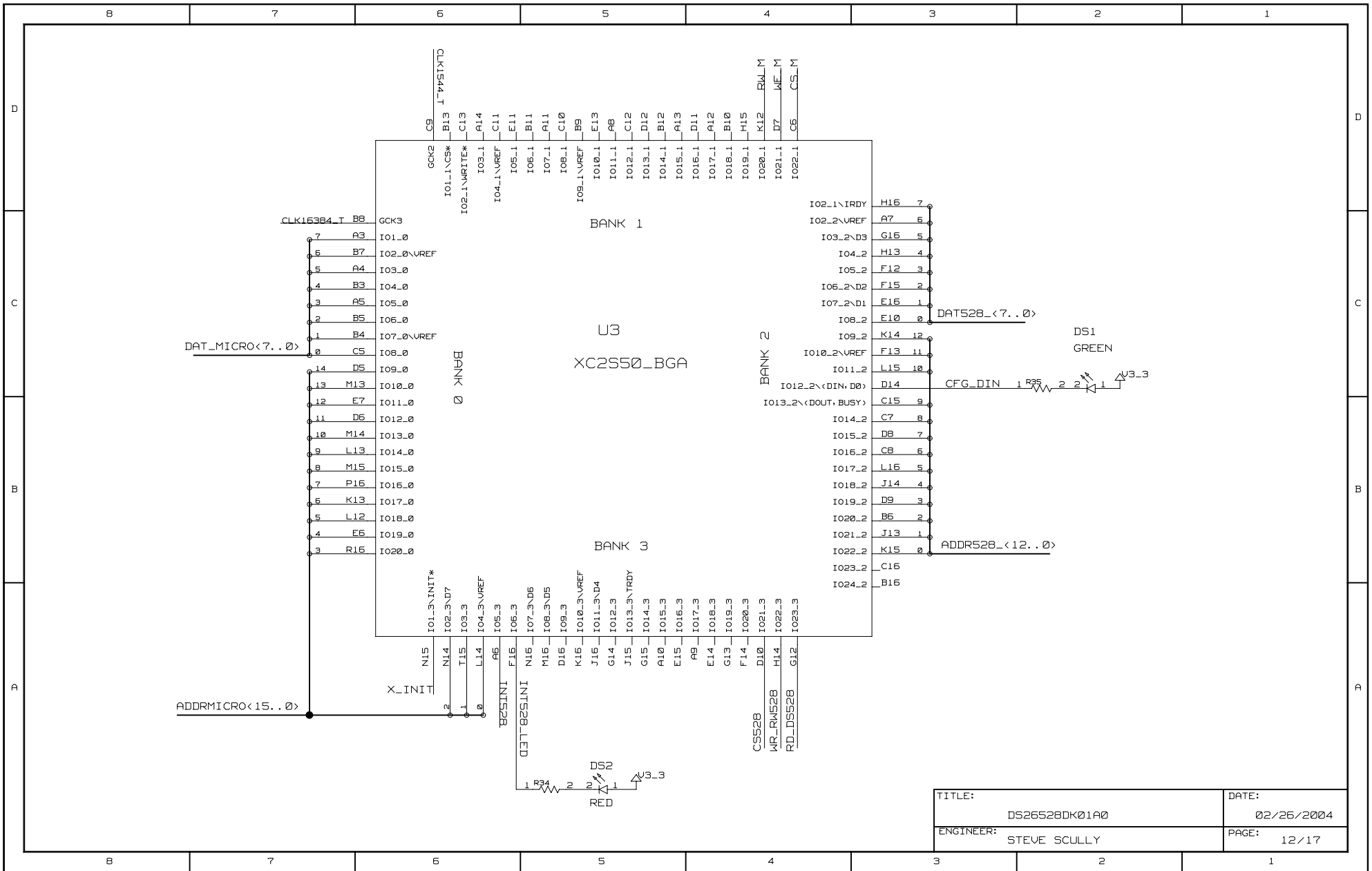
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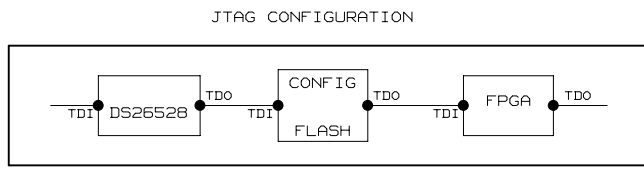
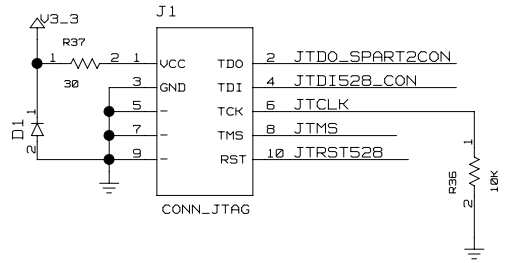
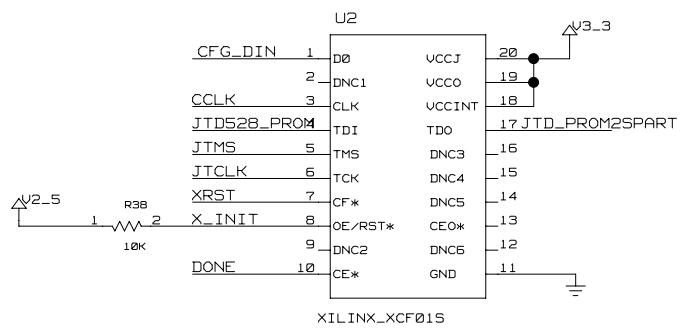
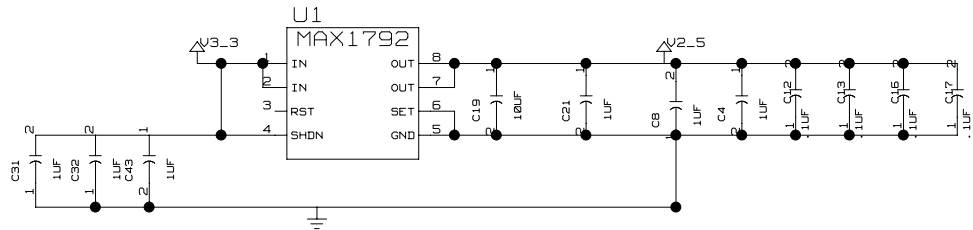
PIN 1, J11 BOTTOM OF BRD  
LEFT SIDE (AS VIEWED FROM BOTTOM)

PCM SIGNALS  
ARE NAMED  
ACCORDING TO  
THE DS26528  
PIN THAT THEY  
CONNECT TO.  
(E.G. PCM\_RXD  
CAN BE DRIVEN BY  
WITH DS26528 RSER)



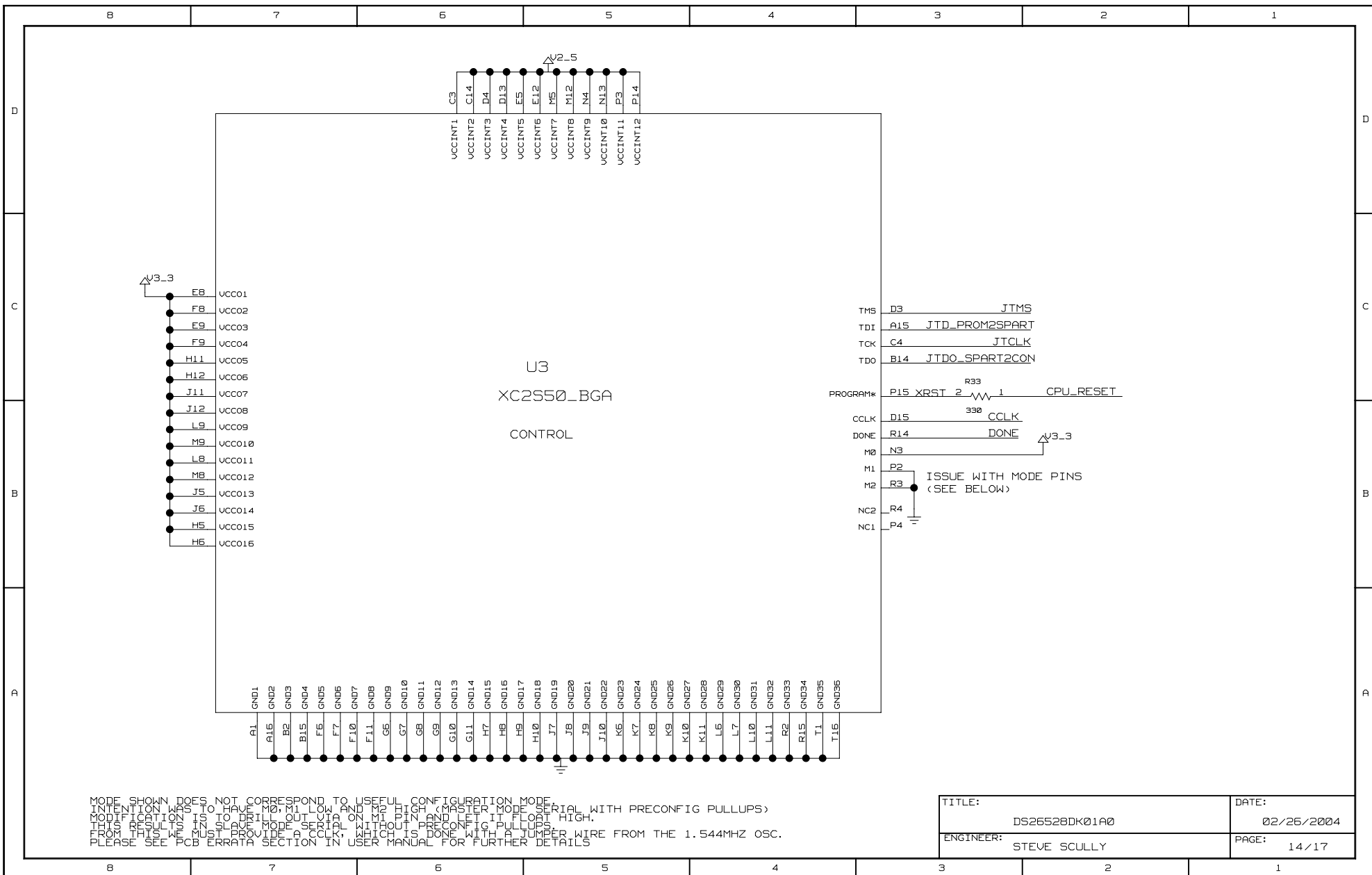
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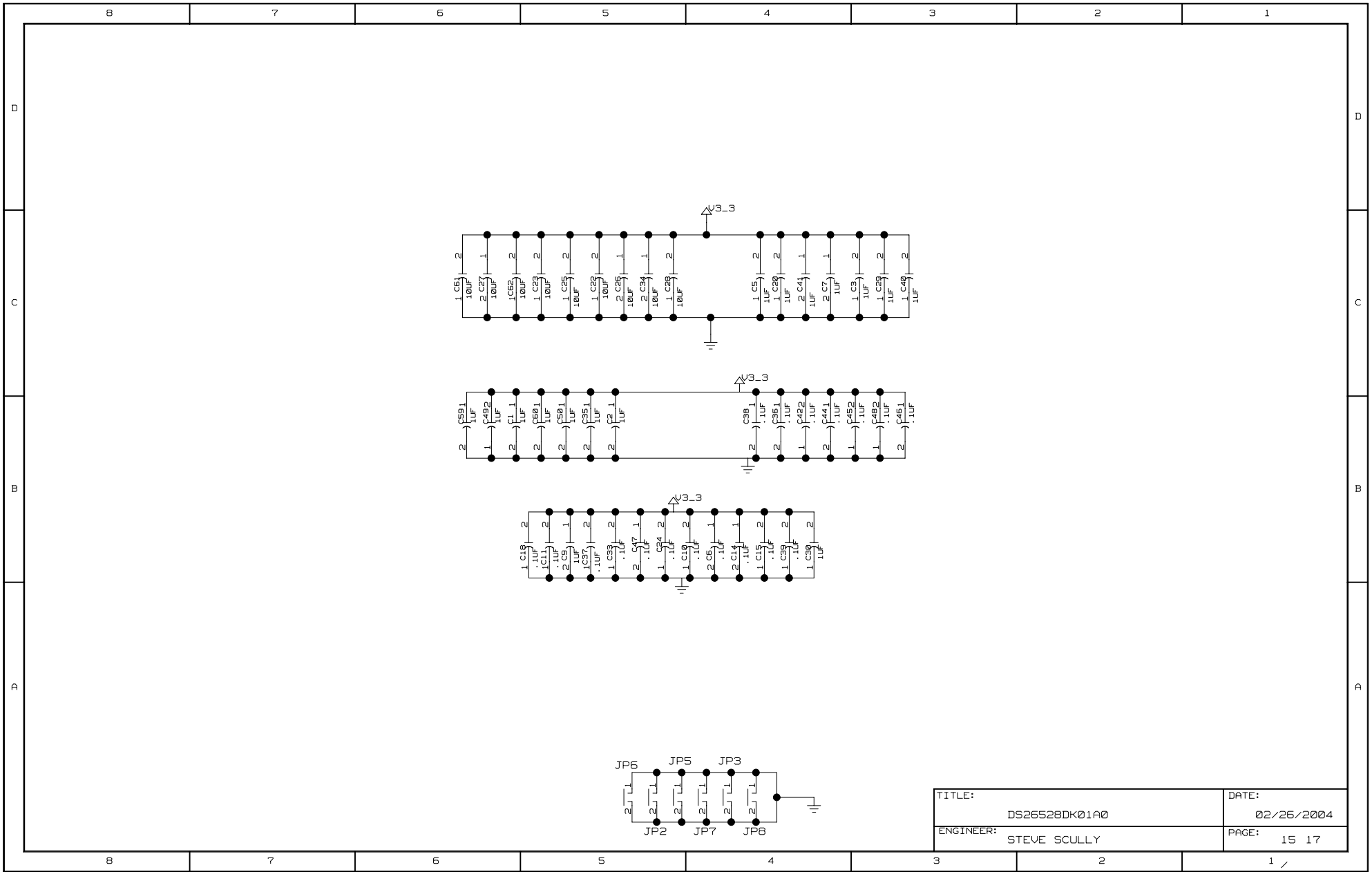
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MODE SHOWN DOES NOT CORRESPOND TO USEFUL CONFIGURATION MODE.  
 INTENTION WAS TO HAVE M0, M1 LOW AND M2 HIGH (MASTER MODE SERIAL WITH PRECONFIG PULLUPS)  
 MODIFICATION IS TO DRILL OUT SERIAL ON M1 PIN AND LET IT FLOAT HIGH.  
 THIS RESULTS IN SLAVE MODE SERIAL WITHOUT PRECONFIG PULLUPS.  
 FROM THIS WE MUST PROVIDE A CCLK, WHICH IS DONE WITH A JUMPER WIRE FROM THE 1.544MHZ OSC.  
 PLEASE SEE PCB ERRATA SECTION IN USER MANUAL FOR FURTHER DETAILS

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|   |   |   |   |   |   |           |       |   |  |
|---|---|---|---|---|---|-----------|-------|---|--|
|   | 8   | 7 | 6   | 5 | 4 | 3         | 2     | 1 |  |
| D | <pre> *** Signal Cross-Reference for the entire design *** ADDRS2B&lt;12..0&gt; 12B2&lt; 2B3 ADDRMICRO&lt;15..0&gt; 11B5&lt; 11B4&lt; 12A8 BPCLKS2B 2B8&lt; 9A6&lt;&gt; 10A3&lt; BTSS2B 2B8&lt; CLK 13C6&lt;&gt; 14B2&lt;&gt; CFG_DIN 12C3&lt;&gt; 13C6&lt;&gt; CLK1544_T 11B2&lt;&gt; 12D6&lt; CLK163B4_T 11B4&lt;&gt; 12C7&lt; CPU_RESET 11B5&lt;&gt; 2B8&lt; 14C2&lt; CS52B 12A4&lt;&gt; 2B8&lt; CS_M 11B7&lt;&gt; 12D4&lt;&gt; DATS2B&lt;7..0&gt; 2A3 12C2 DAT_MICRO&lt;7..0&gt; 11A5&lt; 12C8 DIGIO_ENS2B 9D5&lt;&gt; 2B8&lt; DISINVRX1 5B6&lt;&gt; DISINVRX2 5B2&lt;&gt; DISINVRX3 6B6&lt;&gt; DISINVRX4 5B2&lt;&gt; DISINVRX5 7B6&lt;&gt; DISINVRX6 7B2&lt;&gt; DISINVRX7 8B6&lt;&gt; DISINVRX8 8B2&lt;&gt; DISINVTX1 5C6&lt;&gt; DISINVTX2 5C2&lt;&gt; DISINVTX3 6D6&lt;&gt; DISINVTX4 6D2&lt;&gt; DISINVTX5 7D6&lt;&gt; DISINVTX6 7D2&lt;&gt; DISINVTX7 8D6&lt;&gt; DISINVTX8 8D2&lt;&gt; DONE 13B6&lt;&gt; 14B2&lt;&gt; INTS2B 2B8&lt; 11A7&lt;&gt; 12A6&lt;&gt; INTS2B_LED 12A6&lt;&gt; JTCLK 13A6&lt;&gt; 13B6&lt;&gt; 2C8&lt; 14C2&lt; JTD52B_PROM 2C8&lt; 13C6&lt;&gt; JTD152B_CON 13A5&lt;&gt; 2C8&lt; JTD0_SPART2CON 13A5&lt;&gt; 14C2&lt; JTD_PROM2SPART 13C4&lt;&gt; 14C2&lt; JTM5 13A6&lt;&gt; 13C6&lt;&gt; 2C8&lt; 14C2&lt; JTRSTS2B 13A6&lt;&gt; 2C8&lt; MCLKS2B 9D5&lt;&gt; 10A3&lt;&gt; 2B8&lt; PCM_RSYNC 9A5&lt;&gt; 10D2&lt;&gt; 11C8&lt;&gt; PCM_RXCLK 9A5&lt;&gt; 10D2&lt;&gt; 11C8&lt;&gt; PCM_RXD 9A5&lt;&gt; 10D2&lt;&gt; 11C8&lt;&gt; PCM_TSYNC 9A5&lt;&gt; 10C2&lt;&gt; 11B8&lt;&gt; PCM_TXCLK 9A5&lt;&gt; 10D2&lt;&gt; 11C8&lt;&gt; PCM_TXD 9A5&lt;&gt; 10D2&lt;&gt; 11C8&lt;&gt; RCHBK52B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10D4&lt; 10D6&lt; 10D8&lt; RCLK52B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 9C7&lt; 10A6&lt; 10A8&lt; 10C4&lt; 10C6&lt; 10C8&lt; 10D4&lt; 10D6&lt; 10D8&lt; RD_DSS2B 12A4&lt;&gt; 2B8&lt; REFCLK52B 2B8&lt;&gt; 9A6&lt;&gt; 10A3&lt;&gt; RLFS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 10C8&lt; RLOS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 10B2&lt; RMS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10C4&lt; 10C6&lt; 10C8&lt; RRINGS2B&lt;B..1&gt; 3B4&lt; 3B8&lt; 3D4&lt; 3D8&lt; 4B4&lt; 4B8&lt; 4D4&lt; 4D8&lt; 5B4&lt; 5B8&lt; 6B4&lt; 6B8&lt; 7B4&lt; 7B8&lt; 8B4&lt; 8B8&lt; RSERS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 9B7&lt; 10A6&lt; 10A8&lt; 10C4&lt; 10C6&lt; 10C8&lt; 10D4&lt; 10D6&lt; 10D8&lt; RSIGS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10C4&lt; 10C6&lt; 10C8&lt; RSYNCS2B&lt;B..1&gt; 3A4&lt; 3A8&lt; 3C4&lt; 3C8&lt; 4A4&lt; 4A8&lt; 4C4&lt; 4C8&lt; 9A5 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10D4&lt; 10D6&lt; 10D8&lt; RSYSCLKS2B 9A6&lt;&gt; 10A3&lt;&gt; 2B8&lt; </pre> |   | <pre> RTIPS2B&lt;B..1&gt; 3B4&lt; 3B8&lt; 3C4&lt; 3C8&lt; 4B4&lt; 4B8&lt; 4C4&lt; 4C8&lt; 5B4&lt; 5B8&lt; 6B4&lt; 6B8&lt; 7B4&lt; 7B8&lt; 8B4&lt; 8B8&lt; RW_M 11B6&lt;&gt; 12D4&lt;&gt; SCANENS2B 9D6&lt;&gt; 2C8&lt; SCANMOS2B 9D6&lt;&gt; 2C8&lt; TCHBK52B&lt;B..1&gt; 3A1&lt; 3A5&lt; 3C1&lt; 3C5&lt; 4A1&lt; 4A5&lt; 4C1&lt; 4C5&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10D4&lt; 10D6&lt; 10D8&lt; TCLK52B&lt;B..1&gt; 3B1&lt; 3B5&lt; 3C1&lt; 3C5&lt; 4B1&lt; 4B5&lt; 4C1&lt; 4C5&lt; 9C2&lt; 10A6&lt; 10A8&lt; 10C4&lt; 10C6&lt; 10C8&lt; 10D4&lt; 10D6&lt; 10D8&lt; TRINGS2B&lt;B..1&gt; 3B1&lt; 3B5&lt; 3D1&lt; 3D5&lt; 4B1&lt; 4B5&lt; 4D1&lt; 4D5&lt; 5C4&lt; 5C8&lt; 6C4&lt; 6C8&lt; 7C4&lt; 7C8&lt; 8C4&lt; 8C8&lt; TSERS2B&lt;B..1&gt; 3A1&lt; 3A5&lt; 3C1&lt; 3C5&lt; 4A1&lt; 4A5&lt; 4C1&lt; 4C5&lt; 9B2&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10C8&lt; 10D4&lt; 10D6&lt; 10D8&lt; TSIGS2B&lt;B..1&gt; 3A1&lt; 3A5&lt; 3C1&lt; 3C5&lt; 4A1&lt; 4A5&lt; 4C1&lt; 4C5&lt; 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10C4&lt; 10C6&lt; 10C8&lt; TSSYNC52B 9D5&lt;&gt; 10A3&lt;&gt; 2A8&lt; TSYNCS2B&lt;B..1&gt; 3A1&lt; 3A5&lt; 3C1&lt; 3C5&lt; 4A1&lt; 4A5&lt; 4C1&lt; 4C5&lt; 9D5 10A6&lt; 10A8&lt; 10B4&lt; 10B6&lt; 10B8&lt; 10D4&lt; 10D6&lt; 10D8&lt; TSYSCLKS2B 9D5&lt;&gt; 10A3&lt;&gt; 2B8&lt; TTIPS2B&lt;B..1&gt; 3B1&lt; 3B5&lt; 3C1&lt; 3C5&lt; 4B1&lt; 4B5&lt; 4C1&lt; 4C5&lt; 5D4&lt; 5D8&lt; 6D4&lt; 6D8&lt; 7D4&lt; 7D8&lt; 8D4&lt; 8D8&lt; TXENAS2B 2A8&lt; 9D5&lt;&gt; WE_M 11B6&lt;&gt; 12D4&lt;&gt; WR_RH52B 12A4&lt;&gt; 2B8&lt; XRST 13B6&lt;&gt; 14C3&lt; X_INIT 12A6&lt;&gt; 13B6&lt;&gt; </pre> |   |   |           |       |   |  |
|   | C   |   |   |   |   |           |       |   |  |
| B |   |   |   |   |   |           |       |   |  |
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|   | 8   | 7                          | 6  | 5 | 4 | 3         | 2     | 1 |
| D | <p>*** Part Cross-Reference for the entire design ***</p> |                            |  |   |   |           |       |   |
| C | C1 CAP1 15B6  | D55 LED 10B1               | R27 RES 6D4  |   |   |           |       |   |
|   | C2 CAP1 15B5  | D56 LED 10A1               | R28 RES 6C4  |   |   |           |       |   |
|   | C3 CAP1 15C3  | D57 LED 10B1               | R29 RES 7C8  |   |   |           |       |   |
|   | C4 CAP1 13D5  | D58 LED 10A1               | R30 RES 7D8  |   |   |           |       |   |
|   | C5 CAP1 15C4  | D59 LED 10A1               | R31 RES 8D4  |   |   |           |       |   |
|   | C6 CAP1 15B4  | D510 LED 10B1              | R32 RES 8C4  |   |   |           |       |   |
|   | C7 CAP1 15C4  | D511 LED 10A1              | R33 RES1 14C3  |   |   |           |       |   |
|   | C8 CAP1 13D5  | D512 LED 10B1              | R34 RES1 12A5  |   |   |           |       |   |
|   | C9 CAP1 15B5  | D513 LED 10B1              | R35 RES1 12C2  |   |   |           |       |   |
|   | C10 CAP1 15B4   | D514 LED 10A1              | R36 RES1 13A5  |   |   |           |       |   |
|   | C11 CAP1 15B5   | D515 LED 10A1              | R37 RES1 13B7  |   |   |           |       |   |
|   | C12 CAP1 13D4   | D516 LED 10B1              | R38 RES1 13B6  |   |   |           |       |   |
|   | C13 CAP1 13D4   | D517 LED 10B1              | R39 RES1 10B2  |   |   |           |       |   |
|   | C14 CAP1 15B4   | D518 LED 10A1              | R40 RES1 10A2  |   |   |           |       |   |
|   | C15 CAP1 15B4   | J1 CONN_JTAG 13B7          | R41 RES1 10A1  |   |   |           |       |   |
|   | C16 CAP1 13D4   | J2 CONN_22P 10D5           | R42 RES1 10B1  |   |   |           |       |   |
|   | C17 CAP1 13D4   | J3 CONN_22P 10B7           | R43 RES1 10A1  |   |   |           |       |   |
|   | C18 CAP1 15B5   | J4 CONN_22P 10C7           | R44 RES1 10B1  |   |   |           |       |   |
|   | C19 CAP1 13D6   | J5 CONN_22P 10D7           | R45 RES1 10B2  |   |   |           |       |   |
|   | C20 CAP1 15C4   | J6 CONN_22P 10C3           | R46 RES1 10A2  |   |   |           |       |   |
|   | C21 CAP1 13D5   | J7 CONN_22P 10D3           | R47 RES1 10B1  |   |   |           |       |   |
|   | C22 CAP1 15C5   | J8 CONN_22P 10B5           | R48 RES1 10A1  |   |   |           |       |   |
|   | C23 CAP1 15C5   | J9 CONN_22P 10C5           | R49 RES1 10A1  |   |   |           |       |   |
|   | C24 CAP1 15B5   | J10 CONN_BNC_SP 5B5        | R50 RES1 10B1  |   |   |           |       |   |
|   | C25 CAP1 15C5   | J11 CONN_BNC_SP 5B1        | R51 RES1 10B1  |   |   |           |       |   |
|   | C26 CAP1 15C5   | J12 CONN_BNC_SP 6B5        | R52 RES1 10A1  |   |   |           |       |   |
|   | C27 CAP1 15C5   | J13 CONN_BNC_SP 6B1        | R53 RES1 10A1  |   |   |           |       |   |
|   | C28 CAP1 15C5   | J14 CONN_BNC_SP 7B5        | R54 RES1 10B1  |   |   |           |       |   |
|   | C29 CAP1 15C3   | J15 CONN_BNC_SP 7B1        | R55 RES1 2B9   |   |   |           |       |   |
|   | C30 CAP1 15B4   | J16 CONN_BNC_SP 8B5        | R56 RES1 8A3   |   |   |           |       |   |
|   | C31 CAP1 13D8   | J17 CONN_BNC_SP 8B1        | R57 RES1 8A4   |   |   |           |       |   |
|   | C32 CAP1 13D7   | J18 CONN_BNC_SP 5D5        | R58 RES1 8A7   |   |   |           |       |   |
|   | C33 CAP1 15B5   | J19 CONN_BNC_SP 5D1        | R59 RES1 8A8   |   |   |           |       |   |
|   | C34 CAP1 15C5   | J20 CONN_BNC_SP 6D5        | R60 RES1 7A4   |   |   |           |       |   |
|   | C35 CAP1 15B5   | J21 CONN_BNC_SP 6D1        | R61 RES1 7A3   |   |   |           |       |   |
|   | C36 CAP1 15B4   | J22 CONN_BNC_SP 7D5        | R62 RES1 7A7   |   |   |           |       |   |
|   | C37 CAP1 15B5   | J23 CONN_BNC_SP 7D1        | R63 RES1 7A8   |   |   |           |       |   |
|   | C38 CAP1 15B4   | J24 CONN_BNC_SP 6D5        | R64 RES1 6A3   |   |   |           |       |   |
|   | C39 CAP1 15B4   | J25 CONN_BNC_SP 9D1        | R65 RES1 6A4   |   |   |           |       |   |
|   | C40 CAP1 15C3   | J26 RJ45_8 5C2 5C5 6C2 6C6 | R66 RES1 6A7   |   |   |           |       |   |
|   | C41 CAP1 15C4   | J27 RJ45_8 7C2 7C5 8C2 8C6 | R67 RES1 6A8   |   |   |           |       |   |
|   | C42 CAP1 15B4   | J28 CONN_50P2 11D3         | R68 RES1 5A3   |   |   |           |       |   |
|   | C43 CAP1 13D7   | J29 CONN_50P2 11D7         | R69 RES1 5A3   |   |   |           |       |   |
|   | C44 CAP1 15B4   | JP1 CON12P 10B3            | R70 RES1 5A8   |   |   |           |       |   |
|   | C45 CAP1 15B3   | JP2 JMP 15A5               | R71 RES1 5A7   |   |   |           |       |   |
|   | C46 CAP1 15B3   | JP3 JMP 15A4               | R72 RES1 7B1   |   |   |           |       |   |
|   | C47 CAP1 15B5   | JP4 CON12P 10D1            | R73 RES1 8B5   |   |   |           |       |   |
|   | C48 CAP1 15B3   | JP5 JMP 15A5               | R74 RES1 8B1   |   |   |           |       |   |
|   | C49 CAP1 15B6   | JP6 JMP 15A4               | R75 RES1 6B5   |   |   |           |       |   |
|   | C50 CAP1 15B5   | R1 RES 5B7                 | R76 RES1 7B5   |   |   |           |       |   |
|   | C51 CAP 8A3   | R2 RES 5B7                 | R77 RES1 5B1   |   |   |           |       |   |
|   | C52 CAP 8A8   | R3 RES 5B3                 | R78 RES1 6B1   |   |   |           |       |   |
|   | C53 CAP 7A3   | R4 RES 5B3                 | R79 RES1 5B5   |   |   |           |       |   |
|   | C54 CAP 7A8   | R5 RES 6B7                 | SW1 SWITCH_DPDT_SLIDE_6P 6C5                         |   |   |           |       |   |
|   | C55 CAP 6A3   | R6 RES 6B7                 | SW2 SWITCH_DPDT_SLIDE_6P 7C1                         |   |   |           |       |   |
|   | C56 CAP 6A8   | R7 RES 6B3                 | SW3 SWITCH_DPDT_SLIDE_6P 8C5                         |   |   |           |       |   |
|   | C57 CAP 5A3   | R8 RES 6B3                 | SW4 SWITCH_DPDT_SLIDE_6P 8C1                         |   |   |           |       |   |
|   | C58 CAP 5A8   | R9 RES 7B7                 | SW5 SWITCH_DPDT_SLIDE_6P 7C5                         |   |   |           |       |   |
|   | C59 CAP1 15B6   | R10 RES 7B7                | SW6 SWITCH_DPDT_SLIDE_6P 5C1                         |   |   |           |       |   |
|   | C60 CAP1 15B5   | R11 RES 7B3                | SW7 SWITCH_DPDT_SLIDE_6P 5C5                         |   |   |           |       |   |
|   | C61 CAP1 15C6   | R12 RES 7B3                | SW8 SWITCH_DPDT_SLIDE_6P 6C1                         |   |   |           |       |   |
|   | C62 CAP1 15C6   | R13 RES 8B7                | T1 XFMR_1475.U 5B2 5B7 5D3 5D7 6B3 6B7 6D3 6D7       |   |   |           |       |   |
|   | C63 CAP1 6C7  | R14 RES 8B7                | T2 XFMR_1475.U 7B3 7B7 7D3 7D7 8B3 8B7 8D3 8D7       |   |   |           |       |   |
|   | C64 CAP1 5C3  | R15 RES 8B3                | U1 MAX1792 13D6                                      |   |   |           |       |   |
|   | C65 CAP1 8C7  | R16 RES 8B3                | U2 XILINX_XCF015 13C5                                |   |   |           |       |   |
|   | C66 CAP1 7C3  | R17 RES 5D3                | U3 XC2S50_BGA 9C5 12C5 14C5                          |   |   |           |       |   |
|   | C67 CAP1 6C3  | R18 RES 5C3                | U4 DS26S28_BGA.U 2B6 3B3 3B7 3D3 3D7 4B3 4B7 4D3 4D7 |   |   |           |       |   |
|   | C68 CAP1 5C7  | R19 RES 6D8                |  |   |   |           |       |   |
|   | C69 CAP1 8C3  | R20 RES 6C8                |  |   |   |           |       |   |
|   | C70 CAP1 7C7  | R21 RES 7C4                |  |   |   |           |       |   |
|   | D1 DIODE 13A7   | R22 RES 7D4                |  |   |   |           |       |   |
|   | D51 LED 12C2  | R23 RES 8C8                |  |   |   |           |       |   |
|   | D52 LED 12A5  | R24 RES 8D8                |  |   |   |           |       |   |
|   | D53 LED 10A1  | R25 RES 5C8                |  |   |   |           |       |   |
|   | D54 LED 10B1  | R26 RES 5D8                |  |   |   |           |       |   |
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